The documentation and process conversion measures necessary to comply with this document shall be completed by 15 May 2015.

INCH-POUND

MIL-PRF-19500/406M
27 March 2015
SUPERSEDING
MIL-PRF-19500/406L
3 March 2014

PERFORMANCE SPECIFICATION SHEET

* RECTIFIER, SEMICONDUCTOR DEVICE, SILICON, VOLTAGE REGULATOR, ENCAPSULATED THROUGH-HOLE AND SURFACE MOUNT PACKAGES, DEVICE TYPES 1N4460 THROUGH 1N4496, AND 1N6485 THROUGH 1N6491, QUALITY LEVELS JAN, JANTX, JANTXV, AND JANS

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of this specification sheet and MIL–PRF–19500.

1. SCOPE

* 1.1 Scope. This specification covers the performance requirements for micro-miniature 1.5 watt silicon, low leakage, voltage regulator diodes with tolerances of 5 percent, 2 percent, and 1 percent. Four levels of product assurance (JAN, JANTX, JANTXV and JANS) are provided for each encapsulated device type as specified in MIL–PRF–19500.

* 1.2 Package Outlines. The device packages for the encapsulated device types are as follows: DO-41 in accordance with figure 1, surface mount version US in accordance with figure 2, and surface mount version UM in accordance with figure 3.

1.3 Maximum ratings. T_{STG} = $T_{J(max)}$ = -65°C to +175°C. Maximum ratings are as shown in maximum and primary test ratings (see 3.6.2) herein and as follows:

P_T at T_L = +112ºC L = .375 inch (9.53 mm)	P_T at T_{EC} = +145ºC	$P_{T(PCB1)}$ at T_A = +55ºC	$P_{T(PCB2)}$ T_A = +55ºC	P_T At T_{SP} = +25°C	$R_{\theta JL}$ at L = .375 inch (9.52 mm)
1.5 W (1)	1.5 W (2)	0.6 W (3)	1.5 W (4)	1.5 W (5)	42ºC/W (6)

$R_{\theta JEC}$	$R_{\theta JSP}$	$R_{\theta JA(PCB1)}$	$R_{\theta JA(PCB2)}$	Barometric pressure reduced (high altitude operation)
20ºC/W (7)	56°C/W (8)	200ºC/W (3)	80ºC/W (4)	8 mm Hg

Comments, suggestions, or questions on this document should be addressed to DLA Land and Maritime, ATTN: VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to Semiconductor@dla.mil . Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at https://assist.dla.mil .

AMSC N/A

FSC 5961

1.3 Maximum ratings - continued.

(1) Derate: See figure 4 herein.
(2) Derate: See figure 5 herein.
(3) Derate: See figure 6 herein and 6.4.1 (PCB1) herein.
(4) Derate: See figure 7 herein and 6.4.2 (PCB2) herein.
(5) Derate: See figure 8 herein.
(6) See figures 9 and 10 herein.
(7) See figures 11 and 12 herein.
(8) See figure 13 herein.

1.4 Primary electrical characteristics. Primary electrical characteristics are as shown in maximum and primary test ratings (see 3.6.2) and as follows: 3.3 V dc ≤ V_Z ≤ 200 V dc (nominal).

a. 1N4460D through 1N4496D and 1N6485D through 1N6491D are 1 percent voltage tolerance.

b. 1N4460C through 1N4496C and 1N6485C through 1N6491C are 2 percent voltage tolerance.

c. 1N4460 through 1N4496 and 1N6485 through 1N6491 are 5 percent voltage tolerance.
$R_{\theta JL}$ = 42°C/W (max) at L = .375 inch (9.52 mm) (non-surface mount).
$R_{\theta JEC}$ = 20°C/W (max) (surface mount).
For thermal impedance curves, see figures 9, 10, 11, 12 and 13.
$R_{\theta JSP}$ = 56°C/W (max) (UM surface mount).

* 1.5 Part or Identifying Number (PIN). The PIN is in accordance with MIL–PRF–19500, and as specified herein. See 6.5 for PIN construction example and 6.6 for a list of available PINs.

* 1.5.1 JAN brand and quality level designators.

* 1.5.1.1 Encapsulated devices. The quality level designators for encapsulated devices that are applicable for this specification sheet from the lowest to the highest level are as follows: "JAN", "JANTX", "JANTXV", and "JANS"

* 1.5.2 Device type. The designation system for the device types of rectifiers covered by this specification sheet are as follows.

* 1.5.2.1 First number and first letter symbols. The rectifiers of this specification sheet use the first number and letter symbols "1N".

* 1.5.2.2 Second number symbols. The second number symbols for the rectifiers covered by this specification sheet are as follows: "4460" through "4496" and "6485" through "6491".

* 1.5.3 Suffix symbols. The following suffix symbols are incorporated in the PIN as applicable.

* 1.5.3.1 First suffix symbol. The first suffix symbol "C" indicates that the rectifier is a modified version of the approved device type.

* 1.5.3.2 Following suffix symbols. The following suffix symbols are incorporated in the PIN for this specification sheet:

	A blank second suffix symbol indicates a DO-41 through-hole mount package (see figure 1).
C	Indicates a 2 percent voltage tolerance.
D	Indicates a 1 percent voltage tolerance.
US	Indicates a surface mount package (see figure 2).
CUS	Indicates a surface mount package with a 2 percent voltage tolerance.
DUS	Indicates a surface mount package with a 1 percent voltage tolerance.
UM	Indicates a (see figure 3).

* 1.5.4 Lead finish. The lead finishes applicable to this specification sheet are listed on QML–19500.

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3 and 4 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

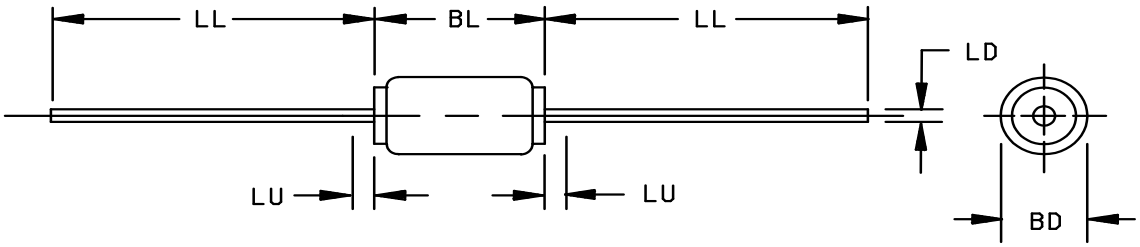
MIL–PRF–19500 - Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL–STD–750 - Test Methods for Semiconductor Devices.

(Copies of these documents are available online at http://quicksearch.dla.mil.)

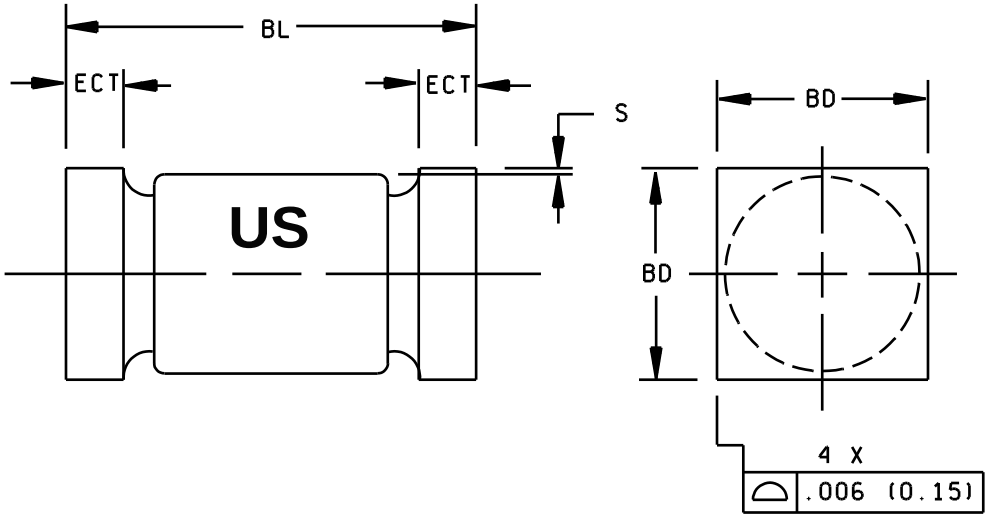
2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.



Ltr	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
BD	.060	.085	1.52	2.16	3
BL	.106	.160	2.69	4.06	3
LD	.028	.032	0.71	0.81	
LL	.800	1.300	20.32	33.02	
LU		.050		1.27	4

NOTES:
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Package contour optional with BD and length BL. Heat slugs, if any, shall be included within this cylinder length but shall not be subject to minimum limit of BD.
4. The specified lead diameters apply in the zone between .050 inch (1.27 mm) from the diode body and the end of the lead.
5. In accordance with ASME Y14.5M, diameters are equivalent to Φx symbology.

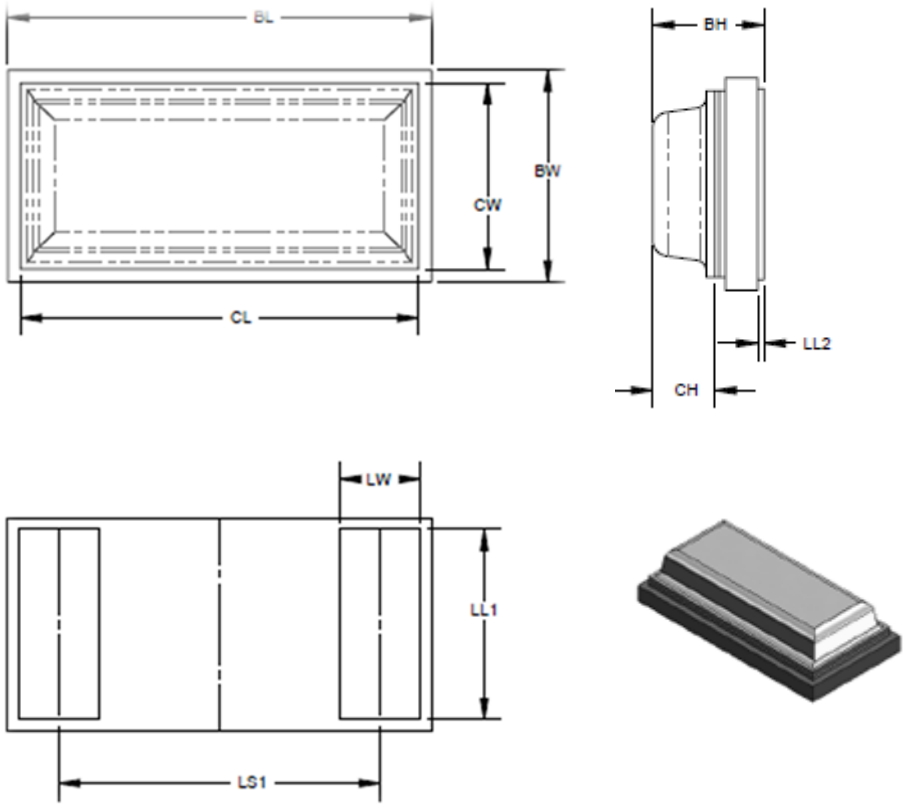
FIGURE 1. Physical dimensions of non-surface mount device (DO-41).



Ltr	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
BD	.091	.103	2.31	2.62
BL	.168	.200	4.28	5.08
ECT	.019	.028	0.48	0.71
S	.003		0.08	

NOTES:
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Dimensions are pre-solder dip.
4. In accordance with ASME Y14.5M, diameters are equivalent to Φx symbology.

FIGURE 2. Physical dimensions of surface mount device (US).



Ltr	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
BL	.192	.202	4.877	5.131
BW	.093	.104	2.362	2.642
BH	.044	.062	1.117	1.574
LW	.030	.044	.762	1.118
LL1	.083	.094	2.108	2.387
LL2	.0024	.0035	.0609	.0889
LS1	.144	.155	3.657	3.937
CH	.020	.034	.508	.864
CL	.179	.191	4.546	4.851
CW	.081	.093	2.057	2.362

FIGURE 3. Physical dimensions of DPC surface mount device, UM.

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in MIL–PRF–19500 and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are authorized by the qualifying activity for listing on the applicable qualified manufacturer's list (QML) before contract award (see 4.2 and 6.3).

3.3 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein shall be as specified in MIL–PRF–19500, and as follows:

EC	End-cap.
IZT	Zener test current.
US	Surface mount case outline, square end-cap.
UM	Surface mount case outline, DPC package.
ZK	Knee impedance.
α_{VZ}	Temperature coefficient.

3.4 Interface and physical dimensions. The interface and physical dimensions shall be as specified in MIL–PRF–19500, and herein. The device package styles shall be as follows: DO-41 in accordance with figure 1, surface mount version US in accordance with figure 2, and surface mount version UM in accordance with figure 3.

3.4.1 Diode construction (except UM version). All devices shall be metallurgically bonded, double plug construction, thermally matched, and non-cavity in accordance with the requirements of MIL–PRF–19500. US version devices shall be structurally identical to the axial leaded type except for lead attachment.

3.4.1.1 Metallurgical bond for diodes with V_Z greater than 6.8 V dc (except UM version). These devices shall be constructed utilizing category I metallurgical bonds for diodes with V_Z greater than 6.8 V dc as defined in MIL–PRF–19500.

3.4.1.2 Metallurgical bond for diodes with V_Z less than or equal to 6.8 V dc (except UM version). These devices shall be constructed utilizing category I or category III metallurgical bonds as defined in MIL–PRF–19500.

3.4.2 Lead finish. Lead finish shall be solderable in accordance with MIL–PRF–19500, MIL–STD–750, and herein. When solder alloy is used for lead finish the maximum lead temperature shall be 175°C max. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see 6.2).

3.5 Marking.

* 3.5.1 Through hole mount packages. Marking shall be in accordance with MIL–PRF–19500.

* 3.5.2 Surface mount packages(US). Marking shall be in accordance with MIL–PRF–19500, except that marking on the US devices shall be marked with a cathode band as a minimum; or a minimum of three evenly spaced contrasting color dots around the periphery of the cathode end may be used. At the option of the manufacturer, US devices may include laser marking on an end-cap, to include part number and lot date code for all levels. JANS devices which are laser marked shall also include serialization. The prefixes JAN, JANTX, JANTXV, or JANS may be abbreviated as J, JX, JV, or JS, respectively. (For example: The part number may be reduced to JS4460). All device marking, except for polarity and serial numbers, shall also appear on the unit package used as the initial protection for delivery.

* 3.5.3 Surface mount packages (UM). Marking shall be in accordance with MIL–PRF–19500, except that marking on the UM version devices only, all marking shall be on lid to include part number, date code, serial number and cathode end.

3.5.4 Polarity. The polarity of all types shall be indicated with a contrasting color band to denote the cathode end. For UM devices, a line on the lid shall denote the cathode end.

3.6 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in 1.3, 1.4, table I and table II herein.

3.6.1 Selection of tighter tolerance devices. The C and D suffix devices shall be selected from JAN, JANTX, JANTXV, or JANS devices, which have successfully completed all applicable screening, and groups A, B, and C testing as ±5 percent tolerance devices. All sublots of C and D suffix devices shall pass table I, subgroup 2, at tightened tolerances. Tighter tolerances for mounting clip temperature shall be maintained for reference purposes to establish correlation. For C and D tolerance levels, T_L = 25°C, +1°C, -3°C at .375 inch (9.53 mm) from body, or zero inches for surface mount devices or equivalent.

3.6.2 Maximum and primary test ratings. Maximum and primary test ratings for voltage regulator diodes are specified in table III herein.

3.7 Workmanship. Devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

a. Qualification inspection (see 4.2).

b. Screening (see 4.3).

c. Conformance inspection (see 4.4).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL–PRF–19500, and as specified herein.

4.2.1 Group E qualification. Group E inspection shall be performed for qualification or requalification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of table II tests, the tests specified in table II herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

* 4.3 Screening (quality levels JANTX, JANTXV and JANS only). Screening of packaged devices shall be in accordance with table E-IV of MIL–PRF–19500, and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen	Measurements	
	JANS level	JANTX and JANTXV levels
3b (1) 3c	Not applicable Thermal impedance, see 4.3.1	Not applicable Thermal impedance, see 4.3.1
9	I_{R1} and V_Z (1N4466 thru 1N4496 only)	Not applicable
10	Required for device > 10 V dc.	Not applicable
11	I_{R1} and V_Z, $\Delta I_{R1} \leq \pm 100$ percent of initial reading or 50 nA, whichever is greater. $\Delta V_Z \leq \pm 2$ percent of initial reading (2)	I_{R1} and V_Z
12	Required see 4.3.2	Required see 4.3.2
13	Scope display see 4.5.7 Subgroups 2 and 3 of table I herein; ΔI_{R1} (max) $\leq \pm 100$ percent of initial reading or 25 percent of column 12 in table III (1N6485 – 1N4466); 50 nA (1N4467 – 1N4496), whichever is greater; $\Delta V_Z \leq \pm 2$ percent of initial reading	Subgroup 2 of table I herein; ΔI_{R1} (max) $\leq \pm 100$ percent of initial reading or 25 percent of column 12 in table III (1N6485 – 1N4466); 50 nA (1N4467 – 1N4496), whichever is greater; $\Delta V_Z \leq \pm 2$ percent of initial reading

(1) Shall be performed any time after temperature cycling, screen 3a; JANTX and JANTXV levels do not need to be repeated in screening requirements.

4.3.1 Thermal impedance. The thermal impedance measurements shall be performed in accordance with method 3101 or 4081 of MIL–STD–750, as applicable, using the guidelines in that method for determining I_M, I_H, t_H, t_{SW} (V_C and V_H where appropriate). See table II, group E, subgroup 4 herein.

4.3.2 Free air power burn-in conditions. Power burn-in conditions are as follows (see 4.5.6): T_A = 75°C maximum. Test conditions in accordance with method 1038 of MIL-STD-750, condition B. Adjust I_Z or T_A to achieve the required T_J, and $I_{Z(min)}$ shall be ≥ 50 percent of column 8 of table III. T_J = 135°C minimum. With approval of the qualifying activity and preparing activity, alternate burn-in criteria (hours, bias conditions, T_J, mounting conditions) may be used for JANTX and JANTXV quality levels. A justification demonstrating equivalence is required. In addition, the manufacturing site's burn-in data and performance history will be essential criteria for burn-in modification approval.

4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL–PRF–19500 and as specified herein.

4.4.1 Group A inspection. Group A inspection shall be in accordance with MIL–PRF–19500 and table I herein.

* 4.4.2 Group B inspection.

* 4.4.2.1 Quality level JANS, table E-VIA of MIL–PRF–19500. Group B inspection shall be conducted in accordance with the tests and conditions specified for subgroup testing in table E-VIA (JANS) of MIL–PRF–19500

Subgroup	Method	Condition
B3	1056	0°C to +100°C, 25 cycles, n = 22, c = 0.
B3	1051	-55°C to +175°C, 100 cycles, n = 22, c = 0.
B3	1071	Fine leak and gross leak shall be performed for UM version devices. Test condition E shall be performed for non-UM version devices. NOTE: For non-transparent devices, hermetic seal may be performed after electrical measurements.
B4	1037	I_Z = 80 percent of column 8 of table III at T_A = room ambient as defined in the general requirements of 4.5 of MIL-STD-750; for 2,000 cycles.
B5	1027	I_Z = 50 percent of column 8 of table III minimum; adjust either T_A, and or I_Z to achieve T_J minimum. Temporary leads may be added for surface mount devices, n = 45, c = 0. Option 1: T_A = +100°C max; T_J = +275°C minimum; t = 96 hours. n = 22, c = 0. Option 2: T_A = +100°C max; T_J = +175°C minimum; t = 1,000 hours. n = 45, c = 0.

* 4.4.2.2 Quality levels JAN, JANTX, and JANTXV of MIL–PRF–19500. Group B inspection shall be conducted in accordance with the tests and conditions specified for subgroup testing in table E-VIB (JAN, JANTX, and JANTXV) of MIL–PRF–19500.

Subgroup	Method	Condition
B2	1056	0°C to +100°C, 10 cycles, n = 22, c = 0.
B2	1051	-55°C to +175°C, 25, cycles, n = 22, c = 0.
B2	1071	Fine leak and gross leak shall be performed for UM version devices. Test condition E shall be performed for non-UM version devices. NOTE: For non-transparent devices, hermetic seal may be performed after electrical measurements.
B3	1027	$I_{Z(min)}$ = 50 percent of column 8 of table III minimum. Adjust either T_A, I_Z, or both to achieve T_J = 150°C min (see 4.5.6).

* 4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in appendix E, table E-VII of MIL–PRF–19500 and herein. Delta requirements shall be in accordance with the applicable inspections of table I, subgroup 2 herein. $Z_{\theta JX}$ is an end-point for these subgroups: C2 and C6 (JAN, JANTX, and JANTXV product levels only).

4.4.3.1 Group C inspection, table E-VII of MIL–PRF–19500.

Subgroup	Method	Condition
C2	1056	0ºC to +100ºC, 15 cycles, n = 22, c = 0.
C2	1051	-55°C to +175°C, 25 cycles, n = 22, c = 0.
C2	1071	Fine leak and gross leak shall be performed for UM suffix devices. Test condition E shall be performed for non-UM suffix devices. NOTE: For non-transparent devices, hermetic seal may be performed after electrical measurements.
C2	2036	Tension - test condition A; 10 lbs; t = 15 s ±3 s. Lead fatigue - Test condition E. NOTE: Not applicable to US and UM suffix devices.
C2	2038	US, URS suffix devices - Tension: Condition B, 10 pounds, t = 15s.
C5	4081	$R_{\theta JL}$ and $R_{\theta JEC}$ see 1.3 and 4.3.2 herein.
C6	1026	$I_{Z(min)}$ = 50 percent of column 8 of table III minimum. Adjust I_Z or T_A to achieve T_J = 150°C min (see 4.5.6).
C7	1018	Not applicable, except for UM suffix devices.
C8	4071	Temperature coefficient for JAN, JANTX, and JANTXV only; I_Z = column 5 of table III; T_{A1} = +25°C ±5°C; T_{A2} = +125°C ±5°C; limit = column 13 of table III (see 4.5.3), n = 22, c = 0.

* 4.4.4 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-IX of MIL–PRF–19500 and as specified in table II herein.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Voltage regulation ($V_{Z(reg)}$). The breakdown voltage shall be measured at I_Z = 10 percent of column 8 of table III and at I_Z = 50 percent of column 8 of table III. The difference between these voltages shall then be determined and shall not exceed column 9 of table III. The voltage measurement at I_Z = 10 percent of column 8 of table III shall be a pulse measurement in accordance with 4.5.5. The measurement at I_Z = 50 percent of column 8 of table III shall be made after current has been applied for 30 ±3 seconds. For this time interval, the device shall be suspended in free air by its leads with mounting clips with inside edge .375 inch (9.53 mm) from the body, and the point of connection shall be maintained at a temperature of +25°C, +8°C, -2°C. No forced air across the device shall be permitted. US suffix devices shall be mounted with the end-caps maintained at +25°C, +8°C, -2°C. For JANHC and JANKC, the die shall be stabilized at +25°C and the test shall be performed utilizing pulse conditions. The ΔV_Z measurement may be performed after a shorter time interval following application of the test current if correlation can be established to the satisfaction of the qualifying activity.

4.5.2 Surge current (I_{ZSM}). The peak currents specified in column 10 of table III shall be applied in the reverse direction and shall be superimposed on the current (I_Z = column 5 of table III) a total of five surges at 1 minute intervals. Each individual surge shall be at one-half square wave pulse of 8.3 millisecond duration or an equivalent sine wave with the same effective (rms) current.

4.5.3 Temperature coefficient of regulator voltage (α_{VZ}). The device shall be temperature stabilized with current applied prior to reading regulator voltage at the specified ambient temperature.

4.5.4 Regulator voltage. The test current (column 5 of table III) shall be applied until thermal equilibrium is attained prior to reading the regulator voltage. For this test, the diode shall be suspended by its leads (non-surface mount) with mounting clips whose inside edge is located at .375 ± .010 inch (9.53 ±0.25 mm) from the body and the lead temperature at inside edge of the mounting clips shall be maintained at a temperature of +23°C to +33°C. For surface mount diodes, the diode shall be suspended by the end-caps with the temperature of the end-caps being maintained at +23°C to +33°C. This measurement may be performed after a shorter time following application of the test current than that which provides thermal equilibrium if correlation to stabilized readings can be established to the satisfaction of the qualifying activity.

4.5.5 Pulse measurements. Conditions for pulse measurements shall be as specified in section 4 of MIL–STD–750.

4.5.6 Free air power burn-in and life tests. The use of a current limiting or ballast resistor is permitted provided that each DUT still sees at least $I_{Z(min)}$ described in 4.3.2 and that the minimum applied voltage, where applicable, is maintained through-out the burn-in period. Use method 3100 of MIL–STD–750 to measure T_J.

4.5.7 Scope display evaluation. Scope display evaluation shall be sharp and stable in accordance with method 4023 of MIL–STD–750. Scope display may be performed on automatic test equipment (ATE) for screening only, with the approval of the qualifying activity. Scope display in table I, subgroup 4 shall be performed on a scope. The reverse current (I_{BR}) over the knee shall be 500 µA peak.

4.5.7.1 Scope display option. At the suppliers option, 100-percent scope display evaluation may be discontinued after three consecutive lots are 100-percent tested with zero failures. Any table I failure shall require 100-percent scope display to be re-invoked.

TABLE I. Group A inspection.

Inspection 1/	MIL–STD–750		Symbol	Limits 2/		Unit
	Method	Conditions		Min	Max	
Subgroup 1						
Visual and mechanical examination	2071					
Subgroup 2						
Thermal impedance	3101	See 4.3.1	$Z_{\theta JX}$			°C/W
Forward voltage	4011	I_F = 200 mA dc	V_{F1}		1.0	V dc
Forward voltage	4011	I_F = 1 A dc	V_{F2}		1.5	V dc
Reverse current leakage	4016	DC method; V_R = column 11 of table III	I_{R1}		Column 12	µA dc
Regulator voltage	4022	I_Z = column 5 of table III (see 4.5.4)	V_Z	Column 3 -5, -2, -1 percent	Column 4 +5, +2, +1 percent	V dc
Subgroup 3						
High temperature operation		T_A = +150°C				
Reverse current leakage	4016	DC method; V_R = column 11 of table III	I_{R2}		Column 15	µA dc
Subgroup 4						
Small-signal reverse breakdown impedance	4051	I_Z = column 5 of table III I_{sig} = 10 percent I_Z	Z_Z		Column 6	ohms
Knee impedance	4051	I_{ZK} = column 14 of table III I_{sig} = 10 percent I_{ZK}	Z_{ZK}		Column 7	ohms
Scope display	4023	See 4.5.7				
Subgroup 5						
Not applicable						
Subgroup 6						
Surge current	4066	I_{ZSM} = column 10 of table III at T_A +25°C (see 4.5.2)	I_{ZSM}		Column 10	A
End-point electrical measurements		See table I, subgroup 2 except $Z_{\theta JX}$				

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection 1/	MIL–PRF–19500		Symbol	Limits 2/		Unit
	Method	Conditions		Min	Max	
Subgroup 7						
Voltage regulation		See 4.5.4	$V_{Z(reg)}$		Column 9	V dc
Temperature coefficient of regulator voltage	4071	JANS level only I_Z = column 5 of table III T_{A1} = +25°C ±5°C, T_{A2} = 120°C ≤ T_2 ≤ 130°C	α_{VZ}		Column 13	%/°C

1/ For sampling plan, see MIL–PRF–19500.
2/ Column references are to table III.

TABLE II. Group E inspection (all quality levels).

Inspection 1/	MIL–STD–750		Sampling plan
	Method	Conditions	
Subgroup 1			22 devices c = 0
Thermal shock	1056	Test condition D, 20 cycles, except low temperature shall be achieved using liquid nitrogen (-195°C). Perform a visual inspection for cracked glass.	
Temp cycling	1051	-65°C to +175°C, 500 cycles.	
Hermetic seal Fine leak Gross leak	1071	Fine leak is applicable for UM version devices only.	
Electrical measurements		See table I, subgroup 2.	
Subgroup 2			22 devices c = 0
Steady-state intermittent operating life	1037	$I_Z = I_{Z2}$ (column 8 of table III) at T_A = room ambient for 10,000 cycles. No forced air cooling on the device shall be permitted.	
Electrical measurements		See table I, subgroup 2.	
Subgroup 4			
Thermal impedance curves		See MIL–PRF–19500.	Sample size N/A
Subgroups 5 and 6			
Not applicable			
Subgroup 8			45 devices c=0
Resistance to glass cracking (Not applicable for UM devices).	1057	Condition B. Step stress to destruction by increased cycles or up to a maximum of 25 cycles.	

1/ A separate sample may be pulled for each test.

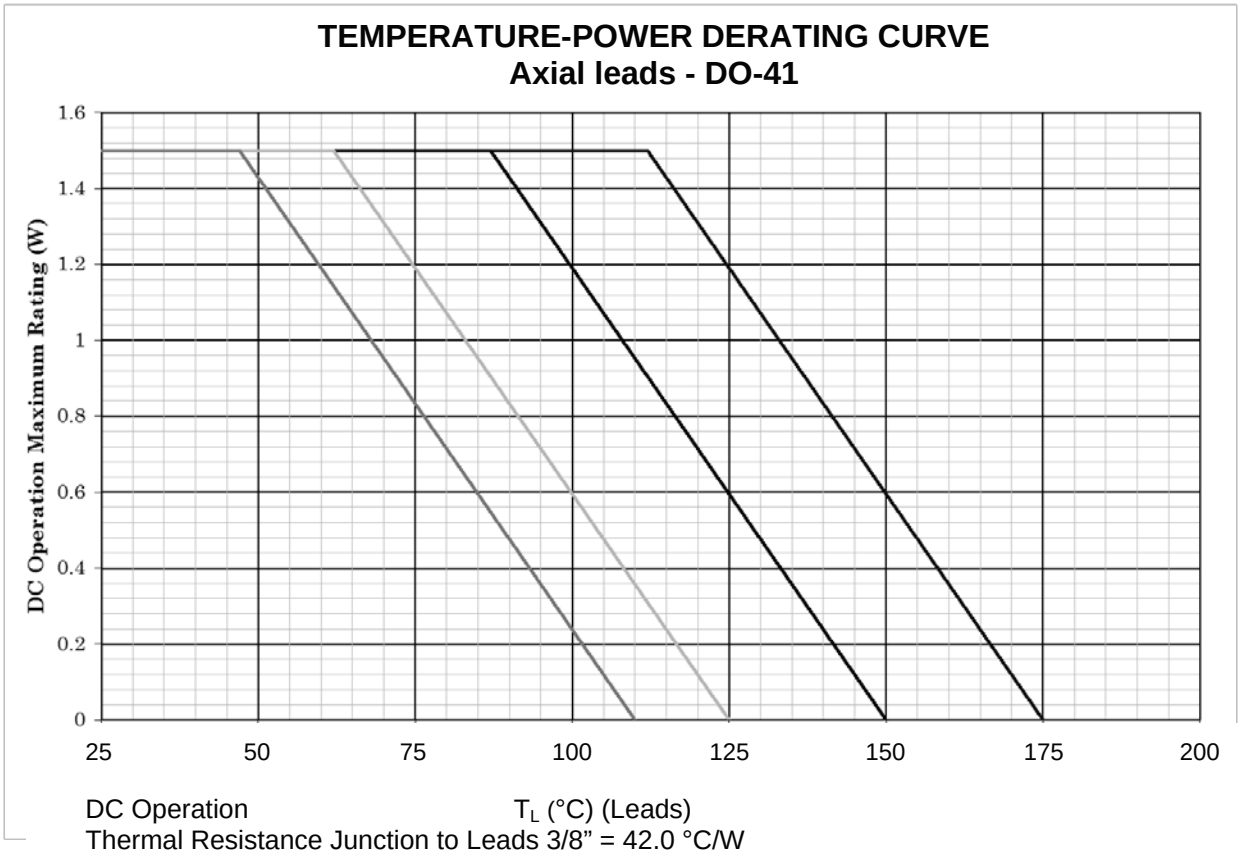
TABLE III. Electrical characteristics and test conditions (all case outlines).

Col 1	Col 2	Col 3	Col 4	Col 5	Col 6	Col 7	Col 8	Col 9	Col 10	Col 11	Col 12	Col 13	Col 14	Col 15
Device type	V_Z Nom	V_Z Min 1/ 2/	V_Z Max 1/ 2/	I_Z test current T_A = +25°C	Z_Z Imped-ance	ZK Knee imped-ance	$I_{Z(max)}$ dc current T_A= +25°C 3/	$V_{Z(reg)}$ Voltage regula-tion 4/	I_{ZSM} T_A = +25°C 5/	V_R Reverse voltage	I_R Reverse current dc I_{R1}	α_{VZ} Temper-ature coefficient 6/	I_{ZK} Test current	I_R T_A = +150°C I_{R2}
	V	V	V	mA	Ω	Ω	mA	V	A	V	µA	%/°C	mA	µA
1N6485	3.3	3.14	3.46	76	10	400	433	0.9	4.2	1.0	50.00	-.075	1.00	500
1N6486	3.6	3.42	3.78	69	10	400	397	0.8	3.9	1.0	50.00	-.070	1.00	200
1N6487	3.9	3.71	4.09	64	9	400	366	.75	3.6	1.0	35.00	-.060	1.00	100
1N6488	4.3	4.09	4.51	58	9	400	332	.70	3.3	1.0	5.00	-.050	1.00	100
1N6489	4.7	4.47	4.93	53	8	500	304	.60	3.0	1.0	4.00	±.025	1.00	100
1N6490	5.1	4.85	5.35	49	7	500	280	.50	2.7	1.0	1.00	±.030	1.00	100
1N6491	5.6	5.32	5.88	45	5	600	255	.40	2.5	2.0	.50	±.040	1.00	100
1N4460	6.2	5.89	6.51	40	4	200	230	.35	2.3	3.72	10.00	+.050	1.00	50
1N4461	6.8	6.46	7.14	37	2.5	200	210	.30	2.1	4.08	5.00	+.057	1.00	20
1N4462	.5	7.13	7.87	34	2.5	400	191	.35	1.9	4.50	1.00	+.061	0.50	10
1N4463	8.2	7.79	8.61	31	3.0	400	174	.40	1.7	4.92	0.50	+.065	0.50	5
1N4464	9.1	8.65	9.55	28	4.0	500	157	.45	1.6	5.46	0.30	+.068	0.50	3
1N4465	10	9.50	10.50	25	5.0	500	143	.50	1.4	8.0	0.30	+.071	0.25	3
1N4466	11	10.45	11.55	23	6.0	550	130	.55	1.3	8.8	0.30	+.073	0.25	2
1N4467	12	11.40	12.60	21	7.0	550	119	.60	1.2	9.6	0.20	+.076	0.25	2
1N4468	13	12.35	13.65	19	8.0	550	110	.65	1.1	10.4	.05	+.079	0.25	2
1N4469	15	14.25	15.75	17	9.0	600	95	.75	.95	12.0	.05	+.082	0.25	2
1N4470	16	15.20	16.80	15.5	10.0	600	90	.80	.90	12.8	.05	+.083	0.25	2
1N4471	18	17.10	18.90	14	11.0	650	79	.83	.79	14.4	.05	+.085	0.25	2
1N4472	20	19.00	21.00	12.5	12.0	650	71	.95	.71	16.0	.05	+.086	0.25	2
1N4473	22	20.90	23.10	11.5	14	650	65	1.0	.65	17.6	.05	+.087	0.25	2
1N4474	24	22.80	25.20	10.5	16	700	60	1.1	.60	19.2	.05	+.088	0.25	2
1N4475	27	25.70	28.30	9.5	18	700	53	1.3	.53	21.6	.05	+.090	0.25	2
1N4476	30	28.50	31.50	8.5	20	750	48	1.4	.48	24.0	.05	+.091	0.25	2
1N4477	33	31.40	34.60	7.5	25	800	43	1.5	.43	26.4	.05	+.092	0.25	2

TABLE III. Electrical characteristics and test conditions (all case outlines) - Continued.

Col 1	Col 2	Col 3	Col 4	Col 5	Col 6	Col 7	Col 8	Col 9	Col 10	Col 11	Col 12	Col 13	Col 14	Col 15
Device type	V_Z Nom	V_Z Min 1/ 2/	V_Z Max 1/ 2/	I_Z test current T_A = +25°C	Z_Z Imped-ance	ZK Knee imped-ance	$I_{Z(max)}$ dc current T_A= +25°C 3/	$V_{Z(reg)}$ Voltage regula-tion 4/	I_{ZSM} T_A = +25°C 5/	V_R Reverse voltage	I_R Reverse current dc I_{R1}	α_{VZ} Temper-ature coeffici-ent 6/	I_{ZK} Test current	I_R T_A = +150°C I_{R2}
	V	V	V	mA	Ω	Ω	mA	V	A	V	µA	%/°C	mA	µA
1N4478	36	34.2	37.8	7.0	27	850	40	1.7	.40	28.8	.05	+.093	0.25	2
1N4479	39	37.1	40.9	6.5	30	900	37	1.8	.37	31.2	.05	+.094	0.25	2
1N4480	43	40.9	45.1	6.0	40	950	33	1.9	.33	34.4	.05	+.095	0.25	2
1N4481	47	44.7	49.3	5.5	50	1000	30	2.1	.30	37.6	.05	+.095	0.25	2
1N4482	51	48.5	53.5	5.0	60	1100	28	2.3	.28	40.8	.05	+.096	0.25	2
1N4483	56	53.2	58.8	4.5	70	1300	26	2.5	.26	44.8	.25	+.096	0.25	10
1N4484	62	58.9	65.1	4.0	80	1500	23	2.7	.23	49.6	.25	+.097	0.25	10
1N4485	68	64.6	71.4	3.7	100	1700	21	3.0	.21	54.4	.25	+.097	0.25	10
1N4486	75	71.3	78.7	3.3	130	2000	19	3.3	.19	60.0	.25	+.098	0.25	10
1N4487	82	77.9	86.1	3.0	160	2500	17	3.6	.17	65.6	.25	+.098	0.25	10
1N4488	91	86.5	95.5	2.8	200	3000	16	4.0	.16	72.8	.25	+.099	0.25	10
1N4489	100	95.0	105.0	2.5	250	3100	14	4.4	.14	80.0	.25	+.100	0.25	10
1N4490	110	104.5	115.5	2.3	300	4000	13	5.0	.13	88.0	.25	+.100	0.25	10
1N4491	120	114.0	126.0	2.0	400	4500	12	5.5	.12	96.0	.25	+.100	0.25	10
1N4492	130	123.5	136.5	1.9	500	5000	11	6.0	.11	104	.25	+.100	0.25	10
1N4493	150	142.5	157.5	1.7	700	6000	9.5	7.0	.095	120	.25	+.100	0.25	10
1N4494	160	152	168	1.6	1000	6500	8.9	8.0	.089	128	.25	+.100	0.25	10
1N4495	180	171	189	1.4	1300	7000	7.9	10.0	.079	144	.25	+.100	0.25	10
1N4496	200	190	210	1.2	1500	8000	7.2	12.0	.072	160	.25	+.100	0.25	10

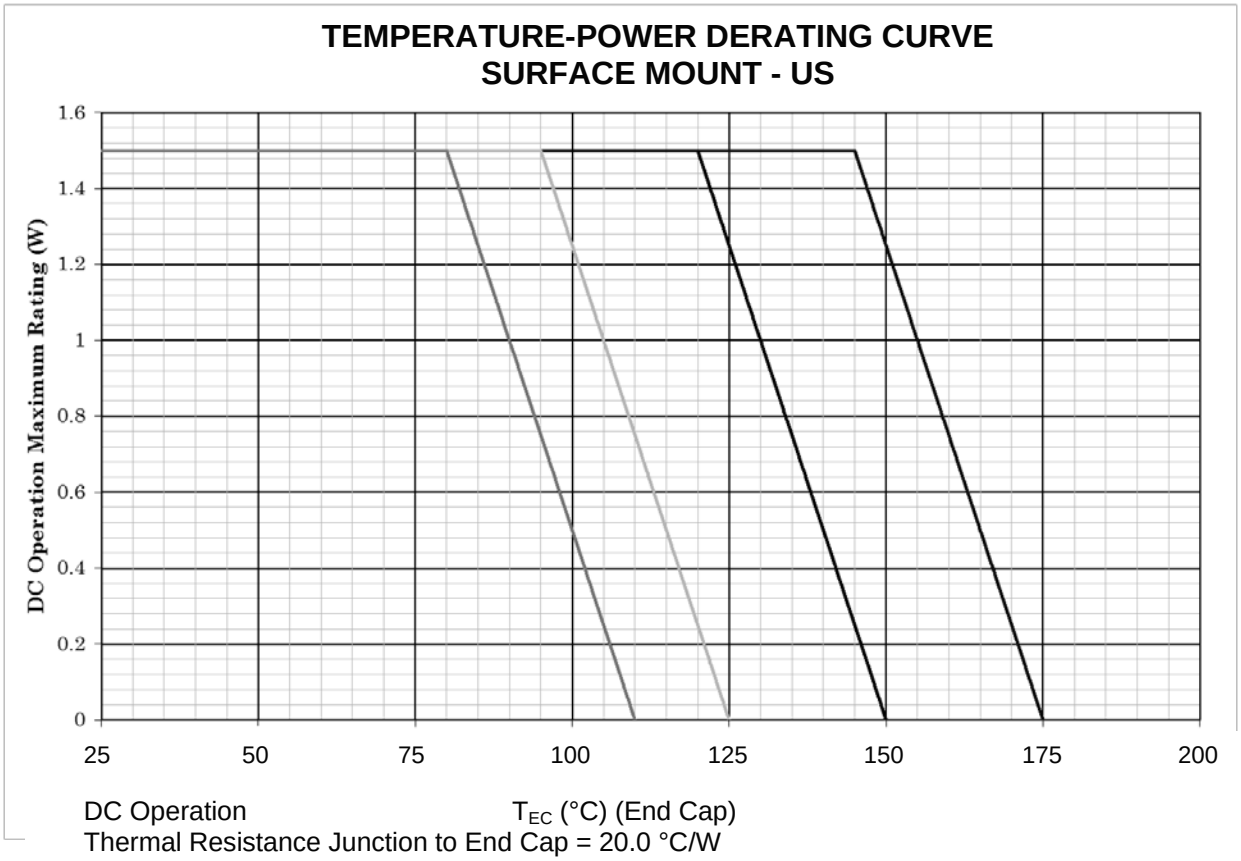
1/ See 4.5.5. Voltages shown are for 5 percent tolerance devices. Voltages for 2 and 1 percent tolerances devices shall be calculated accordingly.
2/ 1N4460D through 1N4496D and 1N6485D through 1N6491D are 1 percent voltage tolerance.
1N4460C through 1N4496C and 1N6485C through 1N6491C are 2 percent voltage tolerance.
1N4460 through 1N4496 and 1N6485 through 1N6491 are 5 percent voltage tolerance.
3/ See 1.3 for P_T temperature conditions for lead, end-cap and UM package where I_{ZM} is applicable.
4/ See 4.5.1.
5/ See 4.5.2.
6/ See 4.5.3.



NOTES:

1. All devices are capable of operating at ≤ T_J specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature (T_J ≤ 175°C) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at T_J ≤ 150°C, where the maximum temperature of electrical test is performed.
4. Derate design curves chosen at T_J ≤ 125°C, and 110°C to show power rating where most users want to limit T_J in their application.

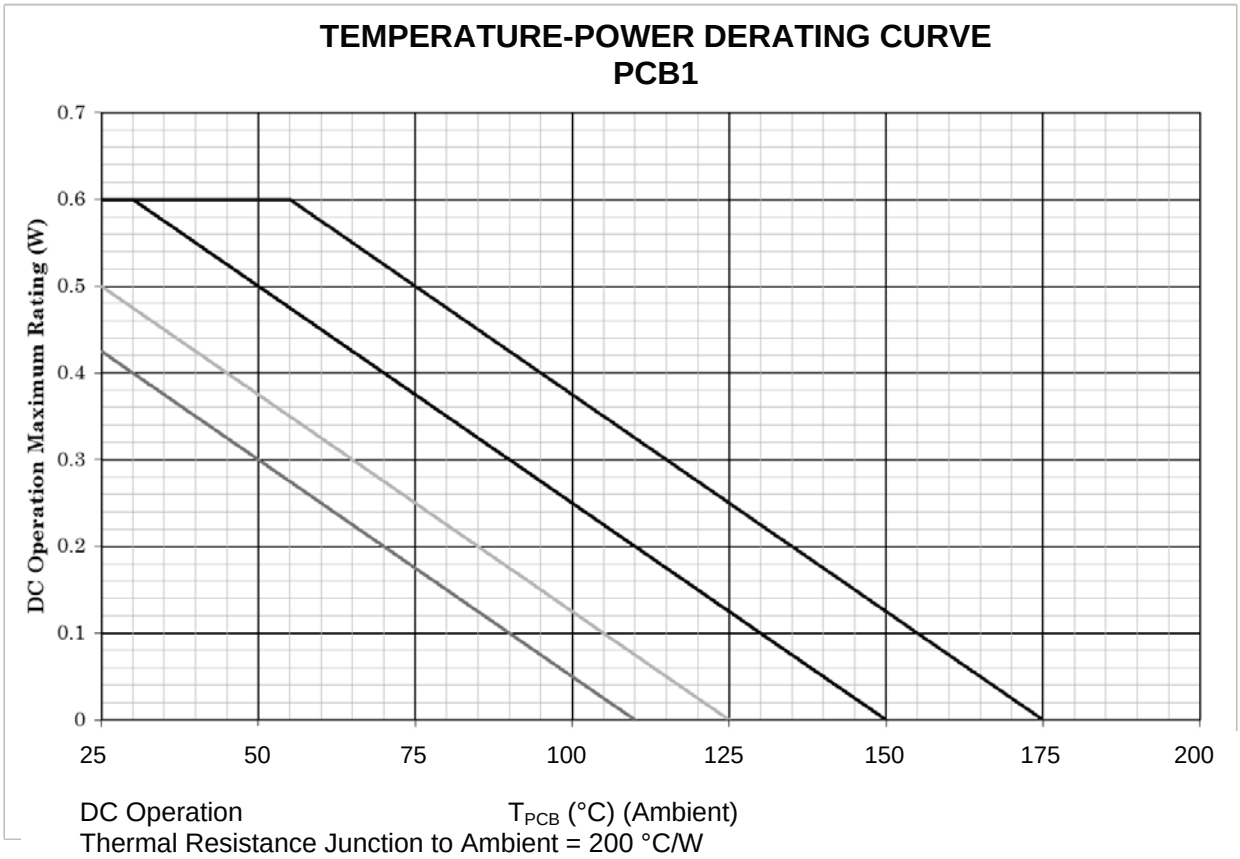
FIGURE 4. Temperature/power derating curve.



NOTES:

1. All devices are capable of operating at ≤ T_J specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature (T_J ≤ 175°C) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at T_J ≤ 150°C, where the maximum temperature of electrical test is performed.
4. Derate design curves chosen at T_J ≤ 125°C, and 110°C to show power rating where most users want to limit T_J in their application.

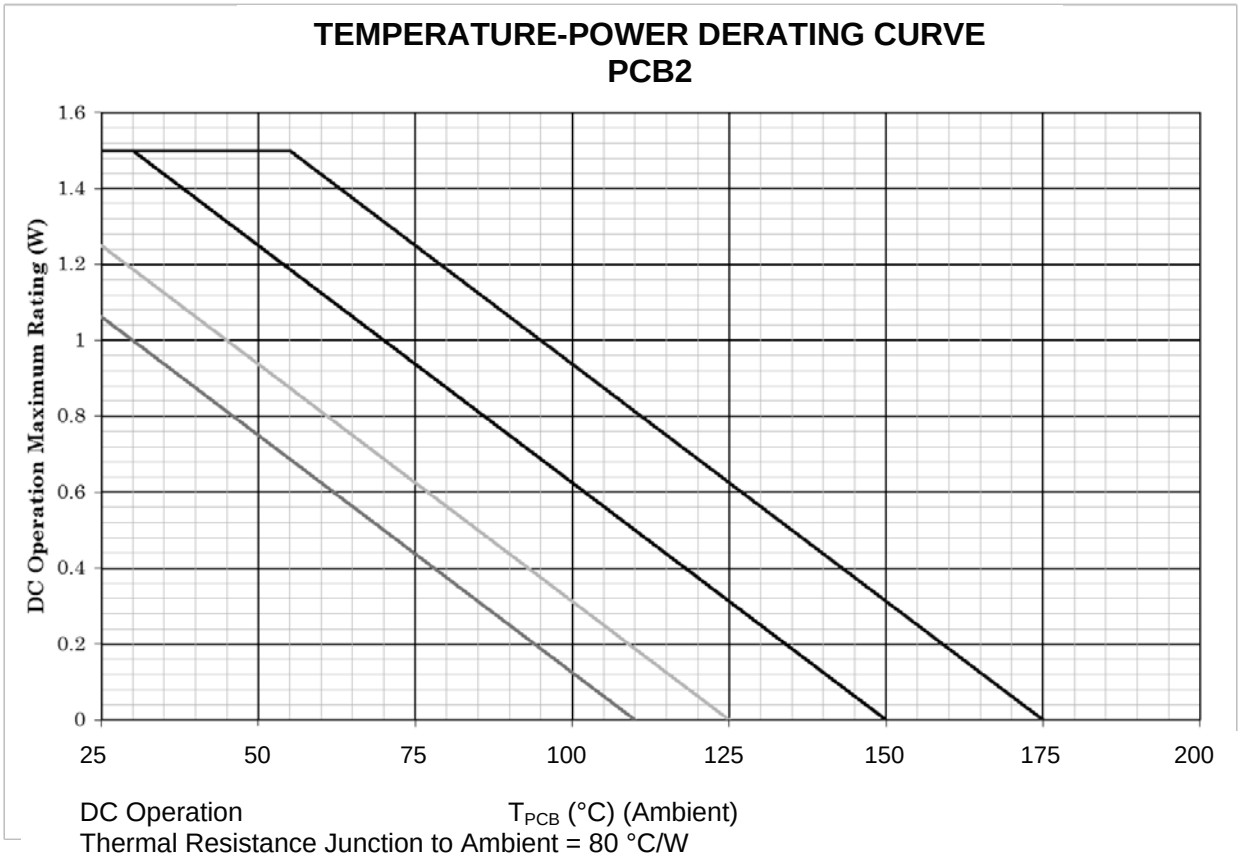
FIGURE 5. Temperature/power derating curve.



NOTES:

1. All devices are capable of operating at ≤ T_J specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature (T_J ≤ 175°C) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at T_J ≤ 150°C, where the maximum temperature of electrical test is performed.
4. Derate design curves chosen at T_J ≤ 125°C, and 110°C to show power rating where most users want to limit T_J in their application.

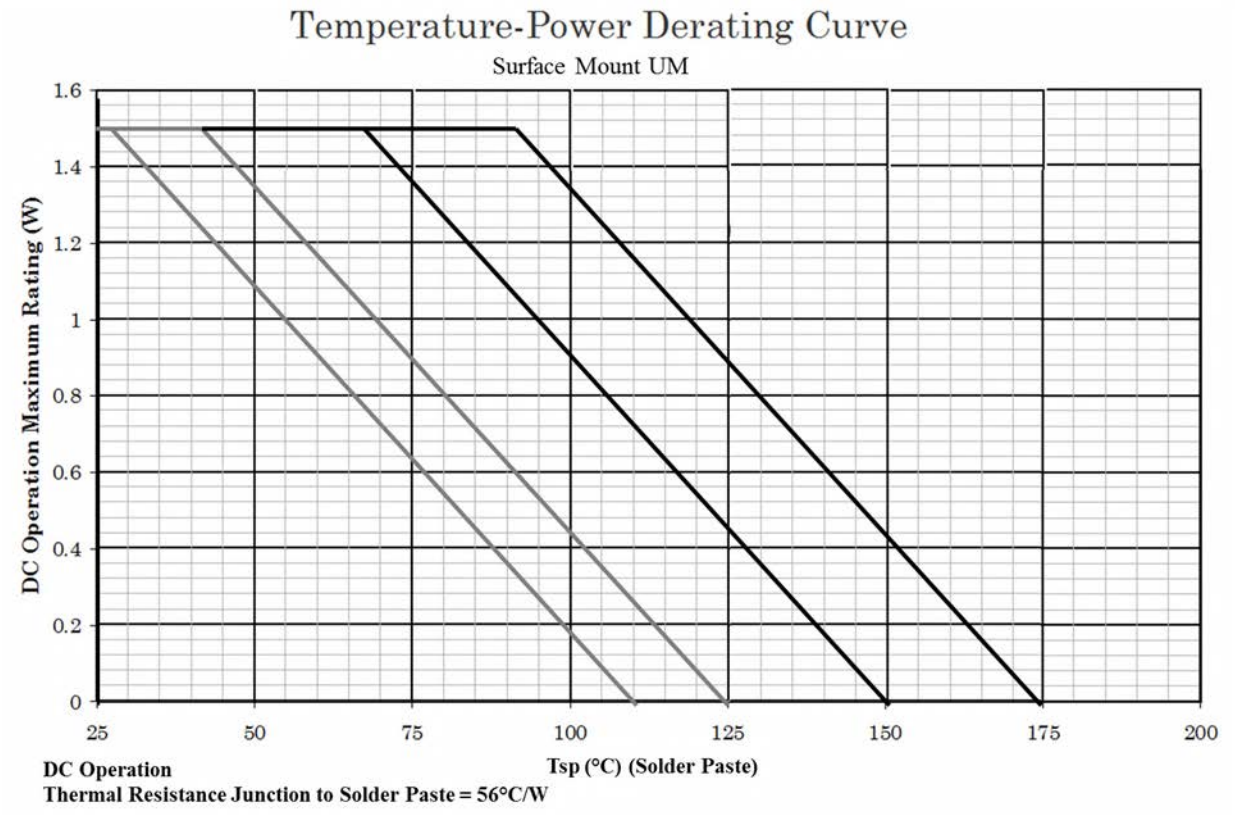
FIGURE 6. Temperature/power derating curve.



NOTES:

1. All devices are capable of operating at ≤ T_J specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature (T_J ≤ 175°C) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at T_J ≤ 150°C, where the maximum temperature of electrical test is performed.
4. Derate design curves chosen at T_J ≤ 125°C, and 110°C to show power rating where most users want to limit T_J in their application.

FIGURE 7. Temperature/power derating curve.



NOTES:

1. All devices are capable of operating at $\leq T_J$ specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature ($T_J \leq 175°C$) and power rating specified. (Ssee 1.3 herein.)
3. Derate design curve chosen at $T_J \leq 150°C$, where the maximum temperature of electrical test is performed.
4. Derate design curves chosen at $T_J \leq 125°C$, and 110°C to show power rating where most users want to limit T_J in their application.

FIGURE 8. Temperature/power derating curve.

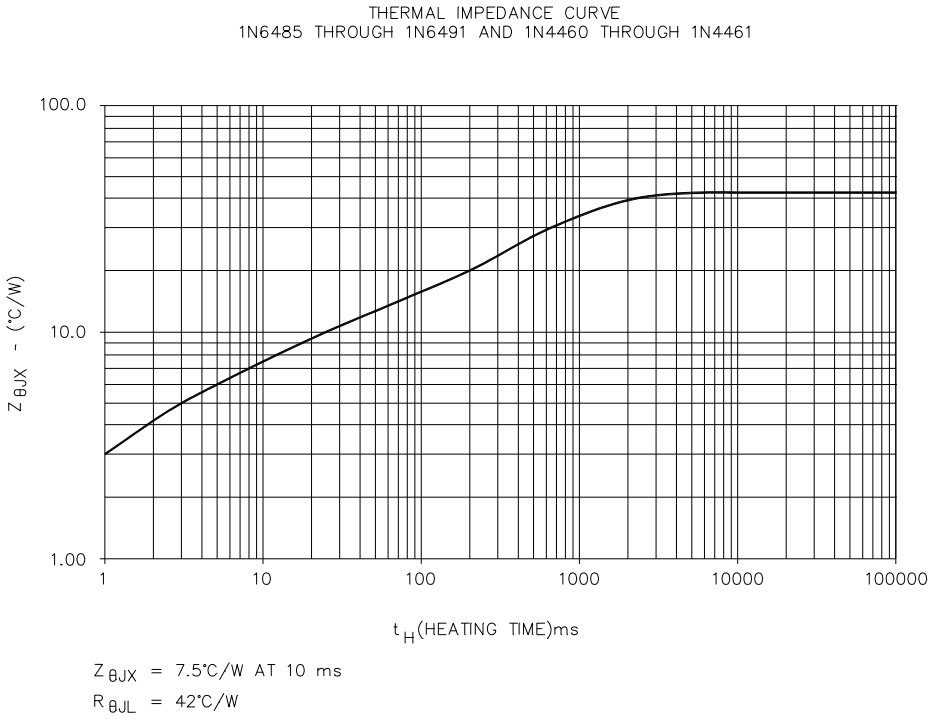
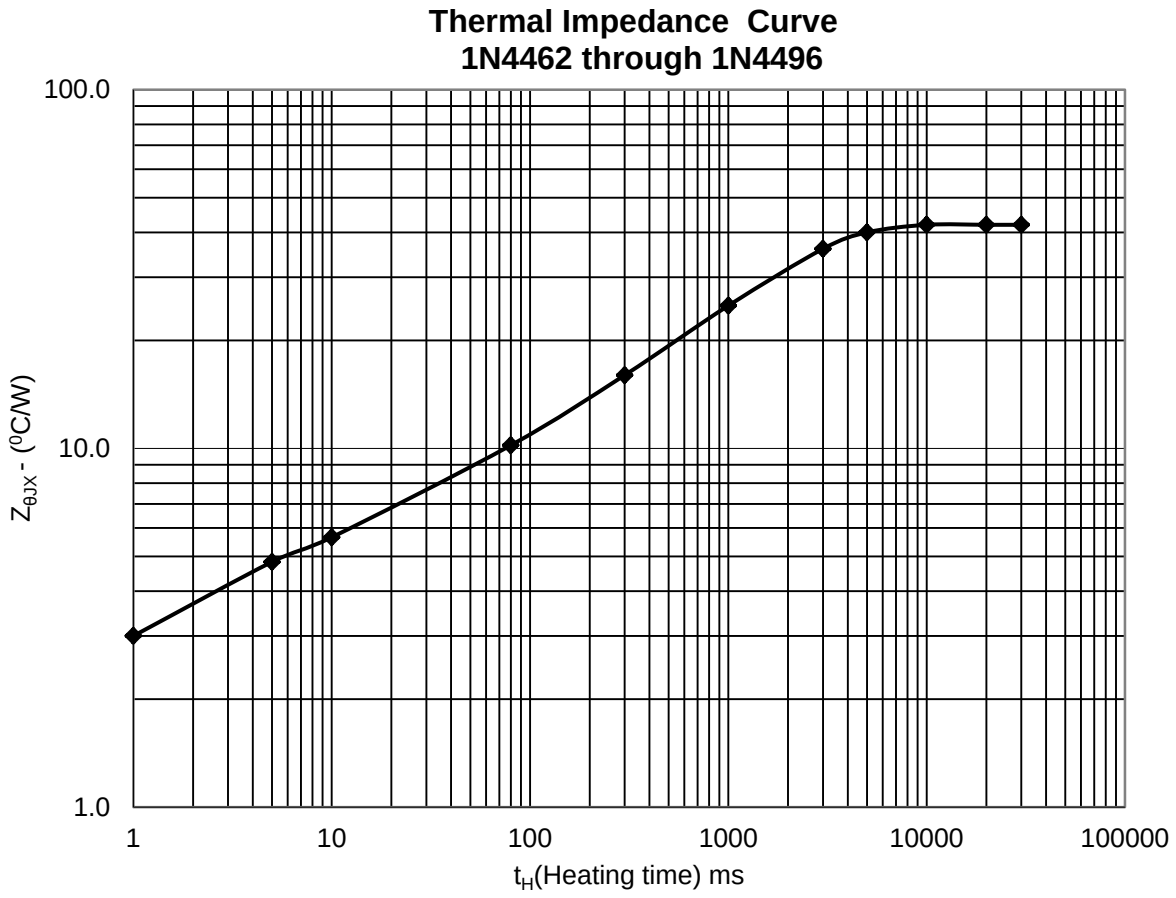


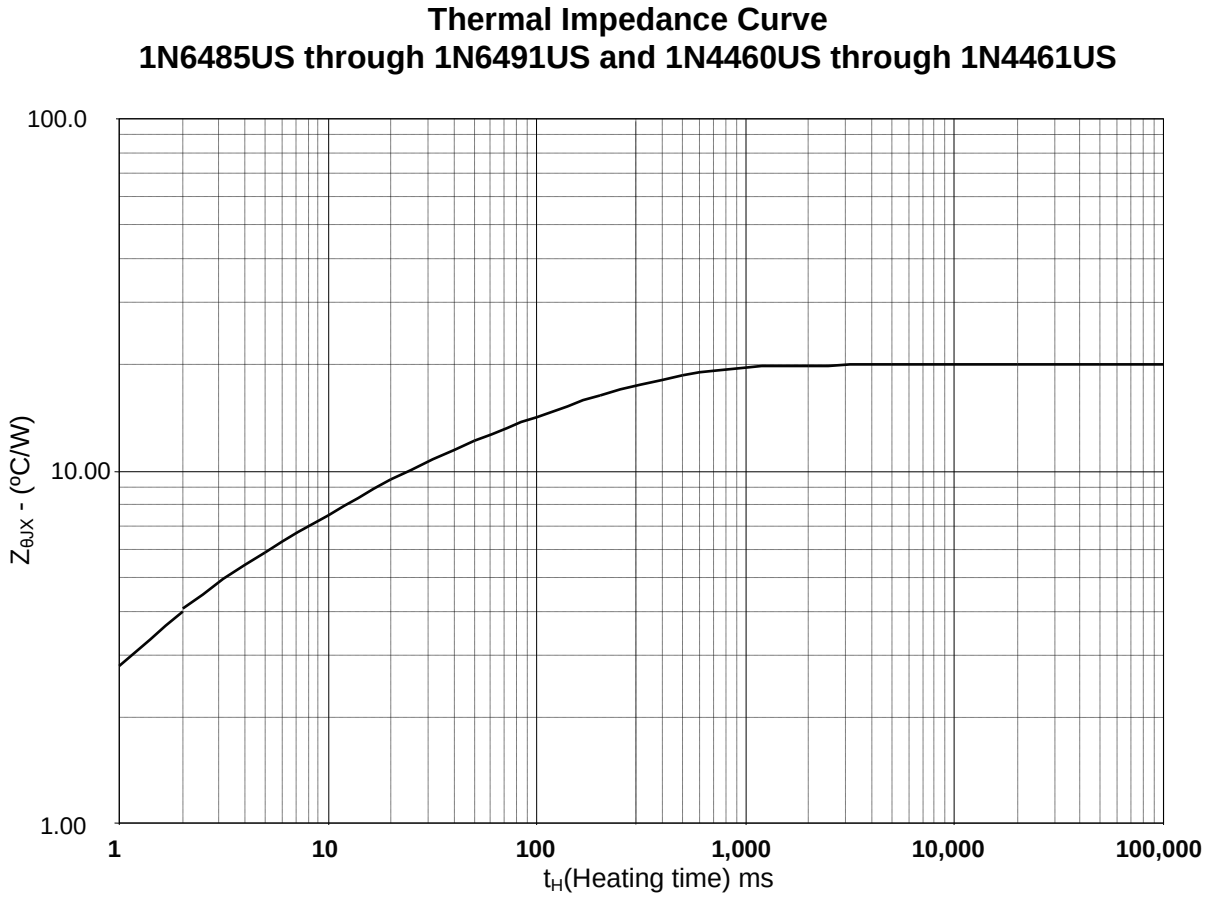
FIGURE 9. Thermal impedance curve for 1N6485 through 1N6491 and 1N4460 through 1N4461.



$Z_{\theta JX}$ = 5.7°C/W at 10 ms

$R_{\theta JL}$ = 42°C/W

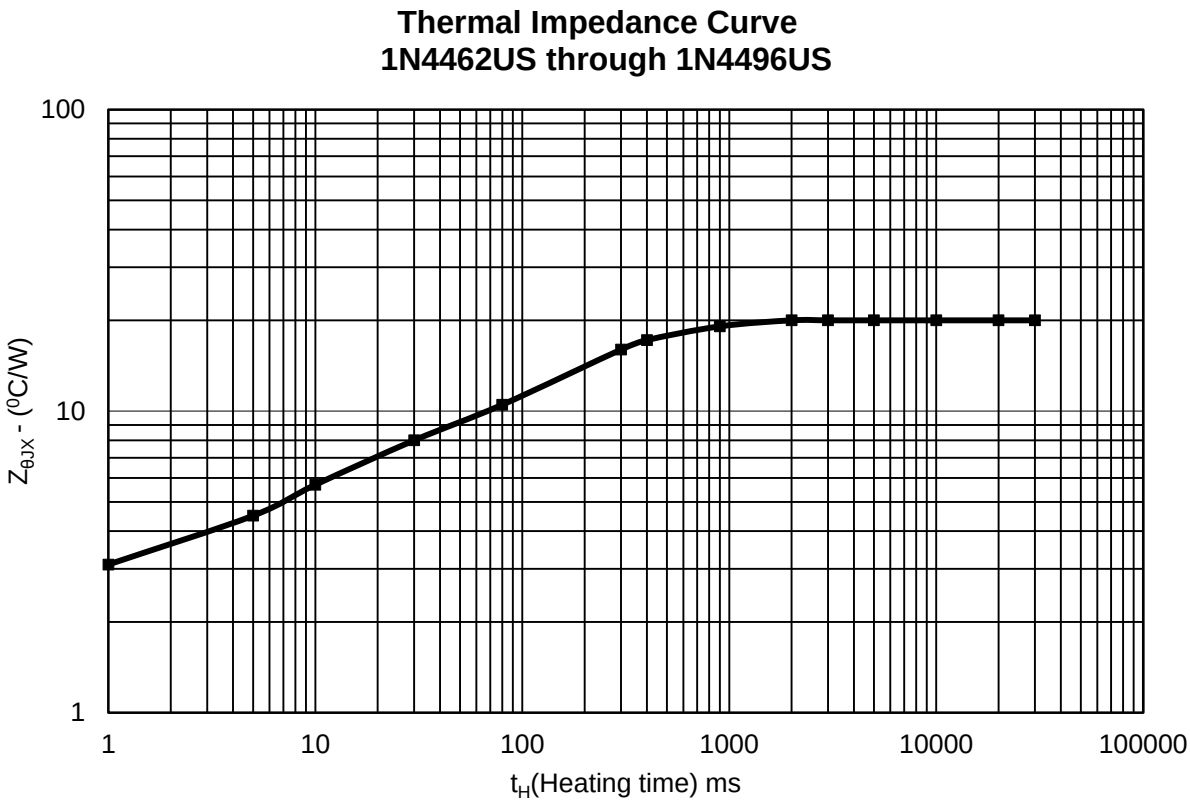
FIGURE 10. Thermal impedance curve for 1N4462 through 1N4496.



$Z_{\theta JX}$ = 7.5°C/W at 10 ms

$R_{\theta JEC}$ = 20°C/W

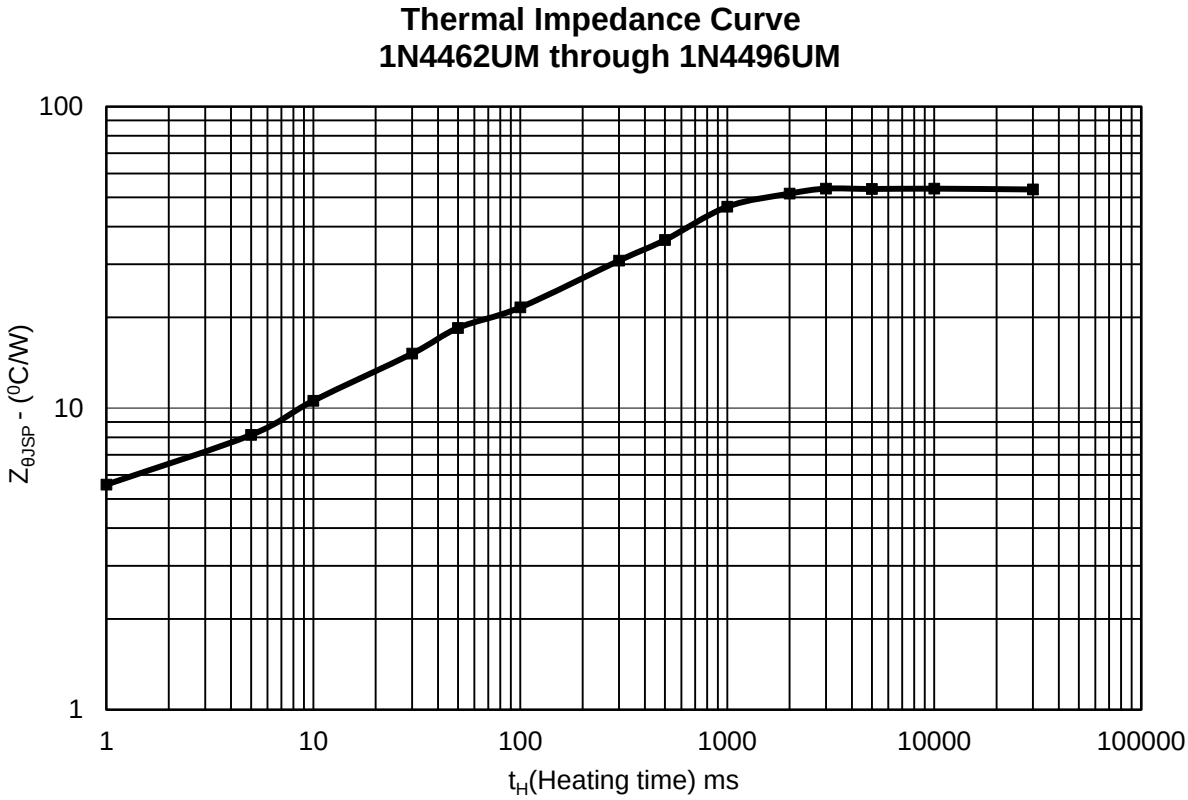
FIGURE 11. Thermal impedance curve for 1N6485US through 1N6491US and 1N4460US through 1N4461US.



$Z_{\theta JX}$ = 5.7°C/W at 10 ms

$R_{\theta JEC}$ = 20°C/W

FIGURE 12. Thermal impedance curve for 1N4462US through 1N4496US.



$Z_{\theta JSP}$ = 10.6 °C/W at 10 ms

$R_{\theta JSP}$ = 56°C/W

NOTE:
1. Curve achieved using 4 in^2 (2,580 mm^2) mounting pad of 2 ounce copper foil.

FIGURE 13. Thermal impedance curve for 1N4462UM through1N4496UM.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in MIL–PRF–19500 are applicable to this specification.)

6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

* 6.2 Acquisition requirements. Acquisition documents should specify the following:

a. Title, number, and date of this specification.

b. Packaging requirements (see 5.1).

c. Lead finish (see 3.4.2).

d. The complete PIN (see 1.5 and 6.5).

e. Surface mount designation if applicable.

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at https://assist.dla.mil.

6.4 Applications data.

6.4.1 PCB (PCB1) mounting with FR4 material for only 0.6 W. For a printed board mounting example with FR4 base material where only 0.6 watts of power is used as shown on figure 6 with 200ºC/W thermal resistance junction to ambient at a T_J of 175ºC and ambient temperature of 55ºC, the following steps guide the user in what the printed board copper mounting pad size will need to be in area for each pad with 1 ounce, 2 ounce, and 3 ounce copper. For axial-leaded, the lead length for mounting will be .187 inch (4.75 mm) or less from body to entry point on PCB surface.

a. Look up thermal resistance value of the required 200°C/W on the Y-axis using a thermal resistance versus copper mounting pad area plot on each of the three curves on figure 15 for different weights of copper foil and then intersect curve horizontally to get the answer. These curves assume still air and horizontal printed board position.

b. In this example, the copper mounting pad sizes for the different copper foil weights would be as follows:

(1) .0085 in^2 (5.48 mm^2) for 1 ounce copper foil.

(2) .0050 in^2 (3.23 mm^2) for 2 ounce copper foil.

(3) .0032 in^2 (2.06 mm^2) for 3 ounce copper foil.

c. Add a conservative guard-band to the copper mounting pad size (larger) to keep T_J below 175ºC.

6.4.2 PCB (PCB2) mounting with FR4 material for the full 1.5 W. For a printed board mounting example with FR4 base material where the full 1.5 watt power rating is used as shown on figure 7 with 80ºC/W thermal resistance junction to ambient at a T_J of 175ºC and ambient temperature of 55ºC, the following steps guide the user in what the printed board copper mounting pad size will need to be in area for each pad with 1 ounce, 2 ounce, and 3 ounce copper. For axial-leaded, the lead length for mounting will be .187 inch (4.75 mm) or less from body to entry point on PCB surface.

a. Look up thermal resistance value of the required 80ºC/W on the Y-axis using a thermal resistance versus copper mounting pad area plot on each of the three curves on figure 15 for different weights of copper foil and then intersect curve horizontally to get the answer. These curves assume still air and horizontal printed board position.

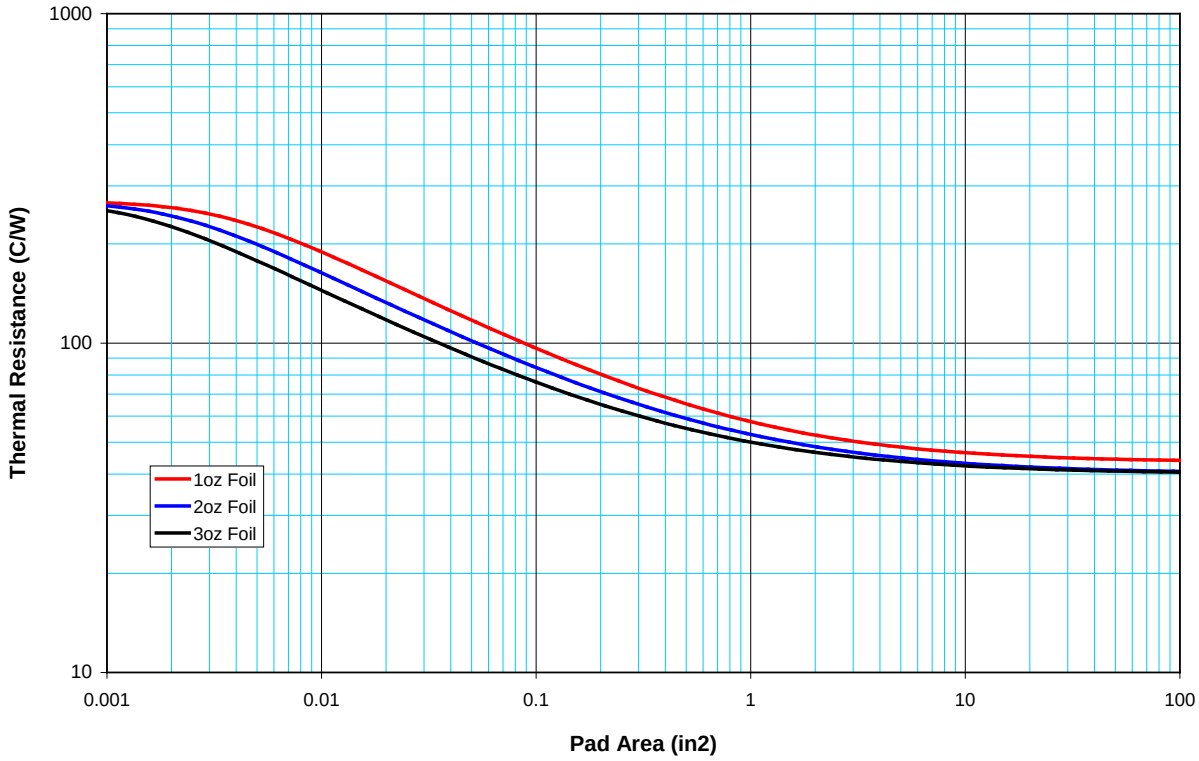
b. In this example the copper mounting pad sizes for the different copper foil weights would be as follows:

(1) .20 in^2 (129 mm^2) for 1 ounce copper foil.

(2) .12 in^2 (77.4 mm^2) for 2 ounce copper foil.

(3) .08 in^2 (51.6 mm^2) for 3 ounce copper foil.

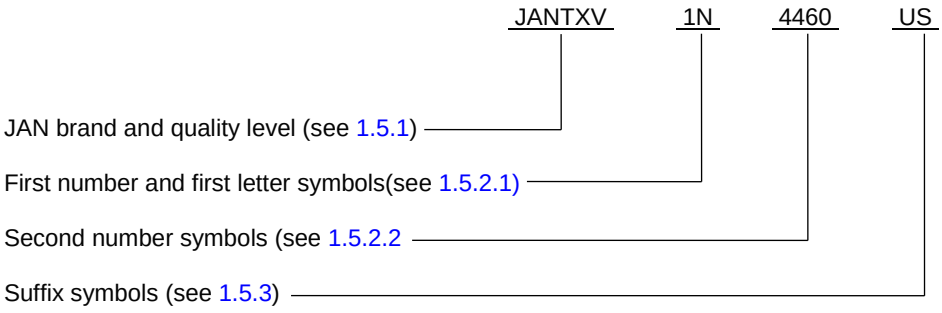
c. Add a conservative guard-band to the copper mounting pad size (larger) to keep T_J below 175ºC.



NOTE:
1. See figure 13 for UM package.

FIGURE 14. Thermal resistance versus FR4 pad area still air, PCB horizontal (for each pad) with 1 oz copper (top curve), 2 oz copper (middle curve), and 3 oz copper (bottom curve).

* 6.5 PIN construction examples. The PIN for encapsulated devices are constructed using the following form.



* 6.6 List of PINs. The following is a list of possible PINs available on this specification sheet.

PINs for devices of the base quality level	PINs for devices of the "TX" quality level	PINs for devices of the "TXV" quality level	PINs for devices of the "S" quality level
JAN1N4460	JANTX1N4460	JANTXV1N4460	JANS1N4460
JAN1N4460C	JANTX1N4460C	JANTXV1N4460C	JANS1N4460C
JAN1N4460CUS	JANTX1N4460CUS	JANTXV1N4460CUS	JANS1N4460CUS
JAN1N4460D	JANTX1N4460D	JANTXV1N4460D	JANS1N4460D
JAN1N4460DUS	JANTX1N4460DUS	JANTXV1N4460DUS	JANS1N4460DUS
JAN1N4460UM	JANTX1N4460UM	JANTXV1N4460UM	JANS1N4460UM
JAN1N4460US	JANTX1N4460US	JANTXV1N4460US	JANS1N4460US
JAN1N4461C	JANTX1N4461C	JANTXV1N4461C	JANS1N4461C
JAN1N4461CUS	JANTX1N4461CUS	JANTXV1N4461CUS	JANS1N4461CUS
JAN1N4461D	JANTX1N4461D	JANTXV1N4461D	JANS1N4461D
JAN1N4461DUS	JANTX1N4461DUS	JANTXV1N4461DUS	JANS1N4461DUS
JAN1N4461UM	JANTX1N4461UM	JANTXV1N4461UM	JANS1N4461UM
JAN1N4461US	JANTX1N4461US	JANTXV1N4461US	JANS1N4461US
JAN1N4462	JANTX1N4462	JANTXV1N4462	JANS1N4462
JAN1N4462C	JANTX1N4462C	JANTXV1N4462C	JANS1N4462C
JAN1N4462CUS	JANTX1N4462CUS	JANTXV1N4462CUS	JANS1N4462CUS
JAN1N4462D	JANTX1N4462D	JANTXV1N4462D	JANS1N4462D
JAN1N4462DUS	JANTX1N4462DUS	JANTXV1N4462DUS	JANS1N4462DUS
JAN1N4462UM	JANTX1N4462UM	JANTXV1N4462UM	JANS1N4462UM
JAN1N4462US	JANTX1N4462US	JANTXV1N4462US	JANS1N4462US
JAN1N4463	JANTX1N4463	JANTXV1N4463	JANS1N4463
JAN1N4463C	JANTX1N4463C	JANTXV1N4463C	JANS1N4463C
JAN1N4463CUS	JANTX1N4463CUS	JANTXV1N4463CUS	JANS1N4463CUS
JAN1N4463D	JANTX1N4463D	JANTXV1N4463D	JANS1N4463D
JAN1N4463DUS	JANTX1N4463DUS	JANTXV1N4463DUS	JANS1N4463DUS
JAN1N4463UM	JANTX1N4463UM	JANTXV1N4463UM	JANS1N4463UM
JAN1N4463US	JANTX1N4463US	JANTXV1N4463US	JANS1N4463US

* 6.6 List of PINs – continued.

JAN1N4464	JANTX1N4464	JANTXV1N4464	JANS1N4464
JAN1N4464C	JANTX1N4464C	JANTXV1N4464C	JANS1N4464C
JAN1N4464CUS	JANTX1N4464CUS	JANTXV1N4464CUS	JANS1N4464CUS
JAN1N4464D	JANTX1N4464D	JANTXV1N4464D	JANS1N4464D
JAN1N4464DUS	JANTX1N4464DUS	JANTXV1N4464DUS	JANS1N4464DUS
JAN1N4464UM	JANTX1N4464UM	JANTXV1N4464UM	JANS1N4464UM
JAN1N4464US	JANTX1N4464US	JANTXV1N4464US	JANS1N4464US
JAN1N4465	JANTX1N4465	JANTXV1N4465	JANS1N4465
JAN1N4465C	JANTX1N4465C	JANTXV1N4465C	JANS1N4465C
JAN1N4465CUS	JANTX1N4465CUS	JANTXV1N4465CUS	JANS1N4465CUS
JAN1N4465D	JANTX1N4465D	JANTXV1N4465D	JANS1N4465D
JAN1N4465DUS	JANTX1N4465DUS	JANTXV1N4465DUS	JANS1N4465DUS
JAN1N4465UM	JANTX1N4465UM	JANTXV1N4465UM	JANS1N4465UM
JAN1N4465US	JANTX1N4465US	JANTXV1N4465US	JANS1N4465US
JAN1N4466	JANTX1N4466	JANTXV1N4466	JANS1N4466
JAN1N4466C	JANTX1N4466C	JANTXV1N4466C	JANS1N4466C
JAN1N4466CUS	JANTX1N4466CUS	JANTXV1N4466CUS	JANS1N4466CUS
JAN1N4466D	JANTX1N4466D	JANTXV1N4466D	JANS1N4466D
JAN1N4466DUS	JANTX1N4466DUS	JANTXV1N4466DUS	JANS1N4466DUS
JAN1N4466UM	JANTX1N4466UM	JANTXV1N4466UM	JANS1N4466UM
JAN1N4466US	JANTX1N4466US	JANTXV1N4466US	JANS1N4466US
JAN1N4467	JANTX1N4467	JANTXV1N4467	JANS1N4467
JAN1N4467C	JANTX1N4467C	JANTXV1N4467C	JANS1N4467C
JAN1N4467CUS	JANTX1N4467CUS	JANTXV1N4467CUS	JANS1N4467CUS
JAN1N4467D	JANTX1N4467D	JANTXV1N4467D	JANS1N4467D
JAN1N4467DUS	JANTX1N4467DUS	JANTXV1N4467DUS	JANS1N4467DUS
JAN1N4467UM	JANTX1N4467UM	JANTXV1N4467UM	JANS1N4467UM
JAN1N4467US	JANTX1N4467US	JANTXV1N4467US	JANS1N4467US
JAN1N4468	JANTX1N4468	JANTXV1N4468	JANS1N4468
JAN1N4468C	JANTX1N4468C	JANTXV1N4468C	JANS1N4468C
JAN1N4468CUS	JANTX1N4468CUS	JANTXV1N4468CUS	JANS1N4468CUS
JAN1N4468D	JANTX1N4468D	JANTXV1N4468D	JANS1N4468D
JAN1N4468DUS	JANTX1N4468DUS	JANTXV1N4468DUS	JANS1N4468DUS
JAN1N4468UM	JANTX1N4468UM	JANTXV1N4468UM	JANS1N4468UM
JAN1N4468US	JANTX1N4468US	JANTXV1N4468US	JANS1N4468US
JAN1N4469	JANTX1N4469	JANTXV1N4469	JANS1N4469
JAN1N4469C	JANTX1N4469C	JANTXV1N4469C	JANS1N4469C
JAN1N4469CUS	JANTX1N469CUS	JANTXV1N4469CUS	JANS1N4469CUS
JAN1N4469D	JANTX1N4469D	JANTXV1N4469D	JANS1N4469D
JAN1N4469DUS	JANTX1N4469DUS	JANTXV1N4469DUS	JANS1N4469DUS
JAN1N4469UM	JANTX1N4469UM	JANTXV1N4469UM	JANS1N4469UM
JAN1N4469US	JANTX1N4469US	JANTXV1N4469US	JANS1N4469US

* 6.6 List of PINs – continued.

JAN1N4470	JANTX1N4470	JANTXV1N4470	JANS1N4470
JAN1N4470C	JANTX1N4470C	JANTXV1N4470C	JANS1N4470C
JAN1N4470CUS	JANTX1N4470CUS	JANTXV1N4470CUS	JANS1N4470CUS
JAN1N4470D	JANTX1N4470D	JANTXV1N4470D	JANS1N4470D
JAN1N4470DUS	JANTX1N4470DUS	JANTXV1N4470DUS	JANS1N4470DUS
JAN1N4470UM	JANTX1N4470UM	JANTXV1N4470UM	JANS1N4470UM
JAN1N4470US	JANTX1N4470US	JANTXV1N4470US	JANS1N4470US
JAN1N4471	JANTX1N4471	JANTXV1N4471	JANS1N4471
JAN1N4471C	JANTX1N4471C	JANTXV1N4471C	JANS1N4471C
JAN1N4471CUS	JANTX1N4471CUS	JANTXV1N4471CUS	JANS1N4471CUS
JAN1N4471D	JANTX1N4471D	JANTXV1N4471D	JANS1N4471D
JAN1N4471DUS	JANTX1N4471DUS	JANTXV1N4471DUS	JANS1N4471DUS
JAN1N4471UM	JANTX1N4471UM	JANTXV1N4471UM	JANS1N4471UM
JAN1N4471US	JANTXN4471US	JANTXV1N4471US	JANS1N4471US
JAN1N4472	JANTX1N4472	JANTXV1N4472	JANS1N4472
JAN1N4472C	JANTX1N4472C	JANTXV1N4472C	JANS1N4472C
JAN1N4472CUS	JANTX1N4472CUS	JANTXV1N4472CUS	JANS1N4472CUS
JAN1N4472D	JANTX1N4472D	JANTXV1N4472D	JANS1N4472D
JAN1N4472DUS	JANTX1N4472DUS	JANTXV1N4472DUS	JANS1N4472DUS
JAN1N4472UM	JANTX1N4472UM	JANTXV1N4472UM	JANS1N4472UM
JAN1N4472US	JANTX1N4472US	JANTXV1N4472US	JANS1N4472US
JAN1N4473	JANTX1N4473	JANTXV1N4473	JANS1N4473
JAN1N4473C	JANTX1N4473C	JANTXV1N4473C	JANS1N4473C
JAN1N4473CUS	JANTX1N4473CUS	JANTXV1N4473CUS	JANS1N4473CUS
JAN1N4473D	JANTX1N4473D	JANTXV1N4473D	JANS1N4473D
JAN1N4473DUS	JANTX1N4473DUS	JANTXV1N4473DUS	JANS1N4473DUS
JAN1N4473UM	JANTX1N4473UM	JANTXV1N4473UM	JANS1N4473UM
JAN1N4473US	JANTX1N4473US	JANTXV1N4473US	JANS1N4473US
JAN1N4474	JANTX1N4474	JANTXV1N4474	JANS1N4474
JAN1N4474C	JANTX1N4474C	JANTXV1N4474C	JANS1N4474C
JAN1N4474CUS	JANTX1N4474CUS	JANTXV1N4474CUS	JANS1N4474CUS
JAN1N4474D	JANTX1N4474D	JANTXV1N4474D	JANS1N4474D
JAN1N4474DUS	JANTX1N4474DUS	JANTXV1N4474DUS	JANS1N4474DUS
JAN1N4474UM	JANTX1N4474UM	JANTXV1N4474UM	JANS1N4474UM
JAN1N4474US	JANTX1N4474US	JANTXV1N4474US	JANS1N4474US
JAN1N4475	JANTX1N4475	JANTXV1N4475	JANS1N4475
JAN1N4475C	JANTX1N4475C	JANTXV1N4475C	JANS1N4475C
JAN1N4475CUS	JANTX1N4475CUS	JANTXV1N4475CUS	JANS1N4475CUS
JAN1N4475D	JANTX1N4475D	JANTXV1N4475D	JANSS1N4475D
JAN1N4475DUS	JANTX1N4475DUS	JANTXV1N4475DUS	JANS1N4475DUS
JAN1N4475UM	JANTX1N4475UM	JANTXV1N4475UM	JANS1N4475UM
JAN1N4475US	JANTX1N4475US	JANTXV1N4475US	JANS1N4475US

* 6.6 List of PINs – continued.

JAN1N4476	JANTX1N4476	JANTXV1N4476	JANS1N4476
JAN1N4476C	JANTX1N4476C	JANTXV1N4476C	JANS1N4476C
JAN1N4476CUS	JANTX1N4476CUS	JANTXV1N4476CUS	JANS1N4476CUS
JAN1N4476D	JANTX1N4476D	JANTXV1N4476D	JANS1N4476D
JAN1N4476DUS	JANTX1N4476DUS	JANTXV1N4476DUS	JANS1N4476DUS
JAN1N4476UM	JANTX1N4476UM	JANTXV1N4476UM	JANS1N4476UM
JAN1N4476US	JANTX1N4476US	JANTXV1N4476US	JANS1N4476US
JAN1N4477	JANTX1N4477	JANTXV1N4477	JANS1N4477
JAN1N4477C	JANTX1N4477C	JANTXV1N4477C	JANS1N4477C
JAN1N4477CUS	JANTX1N4477CUS	JANTXV1N4477CUS	JANS1N4477CUS
JAN1N4477D	JANTX1N4477D	JANTXV1N4477D	JANS1N4477D
JAN1N4477DUS	JANTX1N4477DUS	JANTXV1N4477DUS	JANS1N4477DUS
JAN1N4477UM	JANTX1N4477UM	JANTXV1N4477UM	JANS1N4477UM
JAN1N4477US	JANTX1N4477US	JANTXV1N4477US	JANS1N4477US
JAN1N4478	JANTX1N4478	JANTXV1N4478	JANS1N4478
JAN1N4478C	JANTX1N4478C	JANTXV1N4478C	JANS1N4478C
JAN1N4478CUS	JANTX1N4478CUS	JANTXV1N4478CUS	JANS1N4478CUS
JAN1N4478D	JANTX1N4478D	JANTXV1N4478D	JANS1N4478D
JAN1N4478DUS	JANTX1N4478DUS	JANTXV1N4478DUS	JANS1N4478DUS
JAN1N4478UM	JANTX1N4478UM	JANTXV1N4478UM	JANS1N4478UM
JAN1N4478US	JANTX1N4478US	JANTXV1N4478US	JANS1N4478US
JAN1N4479	JANTX1N4479	JANTXV1N4479	JANS1N4479
JAN1N4479C	JANTX1N4479C	JANTXV1N4479C	JANS1N4479C
JAN1N4479CUS	JANTX1N4479CUS	JANTXV1N4479CUS	JANS1N4479CUS
JAN1N4479D	JANTX1N4479D	JANTXV1N4479D	JANS1N4479D
JAN1N4479DUS	JANTX1N4479DUS	JANTXV1N4479DUS	JANS1N4479DUS
JAN1N4479UM	JANTX1N4479UM	JANTXV1N4479UM	JANS1N4479UM
JAN1N4479US	JANTX1N4479US	JANTXV1N4479US	JANS1N4479US
JAN1N4480	JANTX1N4480	JANTXV1N4480	JANS1N4480
JAN1N4480C	JANTX1N4480C	JANTXV1N4480C	JANS1N4480C
JAN1N4480CUS	JANTX1N4480CUS	JANTXV1N4480CUS	JANS1N4480CUS
JAN1N4480D	JANTX1N4480D	JANTXV1N4480D	JANS1N4480D
JAN1N4480DUS	JANTX1N4480DUS	JANTXV1N4480DUS	JANS1N4480DUS
JAN1N4480UM	JANTX1N4480UM	JANTXV1N4480UM	JANS1N4480UM
JAN1N4480US	JANTX1N4480US	JANTXV1N4480US	JANS1N4480US
JAN1N4481	JANTX1N4481	JANTXV1N4481	JANS1N4481
JAN1N4481C	JANTX1N4481C	JANTXV1N4481C	JANS1N4481C
JAN1N4481CUS	JANTX1N4481CUS	JANTXV1N4481CUS	JANS1N4481CUS
JAN1N4481D	JANTX1N4481D	JANTXV1N4481D	JANS1N4481D
JAN1N4481DUS	JANTX1N4481DUS	JANTXV1N4481DUS	JANS1N4481DUS
JAN1N4481UM	JANTX1N4481UM	JANTXV1N4481UM	JANS1N4481UM
JAN1N4481US	JANTX1N4481US	JANTXV1N4481US	JANS1N4481US

* 6.6 List of PINs – continued.

JAN1N4482	JANTX1N4482	JANTXV1N4482	JANS1N4482
JAN1N4482C	JANTX1N4482C	JANTXV1N4482C	JANS1N4482C
JAN1N4482CUS	JANTX1N4482CUS	JANTXV1N4482CUS	JANS1N4482CUS
JAN1N4482D	JANTX1N4482D	JANTXV1N4482D	JANS1N4482D
JAN1N4482DUS	JANTX1N4482DUS	JANTXV1N4482DUS	JANS1N4482DUS
JAN1N4482UM	JANTX1N4482UM	JANTXV1N4482UM	JANS1N4482UM
JAN1N4482US	JANTX1N4482US	JANTXV1N4482US	JANS1N4482US
JAN1N4483	JANTX1N4483	JANTXV1N4483	JANS1N4483
JAN1N4483C	JANTX1N4483C	JANTXV1N4483C	JANS1N4483C
JAN1N4483CUS	JANTX1N4483CUS	JANTXV1N4483CUS	JANS1N4483CUS
JAN1N4483D	JANTX1N4483D	JANTXV1N4483D	JANS1N4483D
JAN1N4483DUS	JANTX1N4483DUS	JANTXV1N4483DUS	JANS1N4483DUS
JAN1N4483UM	JANTX1N4483UM	JANTXV1N4483UM	JANS1N4483UM
JAN1N4483US	JANTX1N4483US	JANTXV1N4483US	JANS1N4483US
JAN1N4484	JANTX1N4484	JANTXV1N4484	JANS1N4484
JAN1N4484C	JANTX1N4484C	JANTXV1N4484C	JANS1N4484C
JAN1N4484CUS	JANTX1N4484CUS	JANTXV1N4484CUS	JANS1N4484CUS
JAN1N4484D	JANTX1N4484D	JANTXV1N4484D	JANS1N4484D
JAN1N4484DUS	JANTX1N4484DUS	JANTXV1N4484DUS	JANS1N4484DUS
JAN1N4484UM	JANTX1N4484UM	JANTXV1N4484UM	JANS1N4484UM
JAN1N4484US	JANTX1N4484US	JANTXV1N4484US	JANS1N4484US
JAN1N4485	JANTX1N4485	JANTXVTXV1N4485	JANS1N4485
JAN1N4485C	JANTX1N4485C	JANTXV1N4485C	JANS1N4485C
JAN1N4485CUS	JANTX1N4485CUS	JANTXV1N4485CUS	JANS1N4485CUS
JAN1N4485D	JANTX1N4485D	JANTXV1N4485D	JANS1N4485D
JAN1N4485DUS	JANTX1N4485DUS	JANTXV1N4485DUS	JANS1N4485DUS
JAN1N4485UM	JANTX1N4485UM	JANTXV1N4485UM	JANS1N4485UM
JAN1N4485US	JANTX1N4485US	JANTXV1N4485US	JANS1N4485US
JAN1N4486	JANTX1N4486	JANTXV1N4486	JANS1N4486
JAN1N4486C	JANTX1N4486C	JANTXV1N4486C	JANS1N4486C
JAN1N4486CUS	JANTX1N4486CUS	JANTXV1N4486CUS	JANS1N4486CUS
JAN1N4486D	JANTX1N4486D	JANTXV1N4486D	JANS1N4486D
JAN1N4486DUS	JANTX1N4486DUS	JANTXV1N4486DUS	JANS1N4486DUS
JAN1N4486UM	JANTX1N4486UM	JANTXV1N4486UM	JANS1N4486UM
JAN1N4486US	JANTX1N4486US	JANTXV1N4486US	JANS1N4486US
JAN1N4487	JANTX1N4487	JANTXV1N4487	JANS1N4487
JAN1N4487C	JANTX1N4487C	JANTXV1N4487C	JANS1N4487C
JAN1N4487CUS	JANTX1N4487CUS	JANTXV1N4487CUS	JANS1N4487CUS
JAN1N4487D	JANTX1N4487D	JANTXV1N4487D	JANS1N4487D
JAN1N4487DUS	JANTX1N4487DUS	JANTXV1N4487DUS	JANS1N4487DUS
JAN1N4487UM	JANTX1N4487UM	JANTXV1N4487UM	JANS1N4487UM
JAN1N4487US	JANTX1N4487US	JANTXV1N4487US	JANS1N4487US

* 6.6 List of PINs – continued.

JAN1N4488	JANTX1N4488	JANTXV1N4488	JANS1N4488
JAN1N4488C	JANTX1N4488C	JANTXV1N4488C	JANS1N4488C
JAN1N4488CUS	JANTX1N4488CUS	JANTXV1N4488CUS	JANS1N4488CUS
JAN1N4488D	JANTX1N4488D	JANTXV1N4488D	JANS1N4488D
JAN1N4488DUS	JANTX1N4488DUS	JANTXV1N4488DUS	JANS1N4488DUS
JAN1N4488UM	JANTX1N4488UM	JANTXV1N4488UM	JANS1N4488UM
JAN1N4488US	JANTX1N4488US	JANTXV1N4488US	JANS1N4488US
JAN1N4489	JANTX1N4489	JANTXV1N4489	JANS1N4489
JAN1N4489C	JANTX1N4489C	JANTXV1N4489C	JANS1N4489C
JAN1N4489CUS	JANTX1N4489CUS	JANTXV1N4489CUS	JANS1N4489CUS
JAN1N4489D	JANTX1N4489D	JANTXV1N4489D	JANS1N4489D
JAN1N4489DUS	JANTX1N4489DUS	JANTXV1N4489DUS	JANS1N4489DUS
JAN1N4489UM	JANTX1N4489UM	JANTXV1N4489UM	JANS1N4489UM
JAN1N4489US	JANTX1N4489US	JANTXV1N4489US	JANS1N4489US
JAN1N4490	JANTX1N4490	JANTXV1N4490	JANS1N4490
JAN1N4490C	JANTX1N4490C	JANTXV1N4490C	JANS1N4490C
JAN1N4490CUS	JANTX1N4490CUS	JANTXV1N4490CUS	JANS1N4490CUS
JAN1N4490D	JANTX1N4490D	JANTXV1N4490D	JANS1N4490D
JAN1N4490DUS	JANTX1N4490DUS	JANTXV1N4490DUS	JANS1N4490DUS
JAN1N4490UM	JANTX1N4490UM	JANTXV1N4490UM	JANS1N4490UM
JAN1N4490US	JANTX1N4490US	JANTXV1N4490US	JANS1N4490US
JAN1N4491	JANTX1N4491	JANTXV1N4491	JANS1N4491
JAN1N4491C	JANTX1N4491C	JANTXV1N4491C	JANS1N4491C
JAN1N4491CUS	JANTX1N4491CUS	JANTXV1N4491CUS	JANS1N4491CUS
JAN1N4491D	JANTX1N4491D	JANTXV1N4491D	JANS1N4491D
JAN1N4491DUS	JANTX1N4491DUS	JANTXV1N4491DUS	JANS1N4491DUS
JAN1N4491UM	JANTX1N4491UM	JANTXV1N4491UM	JANS1N4491UM
JAN1N4491US	JANTX1N4491US	JANTXV1N4491US	JANS1N4491US
JAN1N4492	JANTX1N4492	JANTXV1N4492	JANS1N4492
JAN1N4492C	JANTX1N4492C	JANTXV1N4492C	JANS1N4492C
JAN1N4492CUS	JANTX1N4492CUS	JANTXV1N4492CUS	JANS1N4492CUS
JAN1N4492D	JANTX1N4492D	JANTXV1N4492D	JANS1N4492D
JAN1N4492DUS	JANTX1N4492DUS	JANTXV1N4492DUS	JANS1N4492DUS
JAN1N4492UM	JANTX1N4492UM	JANTXV1N4492UM	JANS1N4492UM
JAN1N4492US	JANTX1N4492US	JANTXV1N4492US	JANS1N4492US
JAN1N4493	JANTX1N4493	JANTXV1N4493	JANS1N4493
JAN1N4493C	JANTX1N4493C	JANTXV1N4493C	JANS1N4493C
JAN1N4493CUS	JANTX1N4493CUS	JANTXV1N4493CUS	JANS1N4493CUS
JAN1N4493D	JANTX1N4493D	JANTXV1N4493D	JANS1N4493D
JAN1N4493DUS	JANTX1N4493DUS	JANTXV1N4493DUS	JANS1N4493DUS
JAN1N4493UM	JANTX1N4493UM	JANTXV1N4493UM	JANS1N4493UM
JAN1N4493US	JANTX1N4493US	JANTXV1N4493US	JANS1N4493US

* 6.6 List of PINs – continued.

JAN1N4494	JANTX1N4494	JANTXV1N4494	JANS1N4494
JAN1N4494C	JANTX1N4494C	JANTXV1N4494C	JANS1N4494C
JAN1N4494CUS	JANTX1N4494CUS	JANTXV1N4494CUS	JANS1N4494CUS
JAN1N4494D	JANTX1N4494D	JANTXV1N4494D	JANS1N4494D
JAN1N4494DUS	JANTX1N4494DUS	JANTXV1N4494DUS	JANS1N4494DUS
JAN1N4494UM	JANTX1N4494UM	JANTXV1N4494UM	JANS1N4494UM
JAN1N4494US	JANTX1N4494US	JANTXV1N4494US	JANS1N4494US
JAN1N4495	JANTX1N4495	JANTXV1N4495	JANS1N4495
JAN1N4495C	JANTX1N4495C	JANTXV1N4495C	JANS1N4495C
JAN1N4495CUS	JANTX1N4495CUS	JANTXV1N4495CUS	JANS1N4495CUS
JAN1N4495D	JANTX1N4495D	JANTXV1N4495D	JANS1N4495D
JAN1N4495DUS	JANTX1N4495DUS	JANTXV1N4495DUS	JANS1N4495DUS
JAN1N4495UM	JANTX1N4495UM	JANTXV1N4495UM	JANS1N4495UM
JAN1N4495US	JANTX1N4495US	JANTXV1N4495US	JANS1N4495US
JAN1N4496	JANTX1N4496	JANTXV1N4496	JANS1N4496
JAN1N4496C	JANTX1N4496C	JANTXV1N4496C	JANS1N4496C
JAN1N4496CUS	JANTX1N4496CUS	JANTXV1N4496CUS	JANS1N4496CUS
JAN1N4496D	JANTX1N4496D	JANTXV1N4496D	JANS1N4496D
JAN1N4496DUS	JANTX1N4496DUS	JANTXV1N4496DUS	JANS1N4496DUS
JAN1N4496UM	JANTX1N4496UM	JANTXV1N4496UM	JANS1N4496UM
JAN1N4496US	JANTX1N4496US	JANTXV1N4496US	JANS1N4496US
JAN1N6485	JANTX1N6485	JANTXV1N6485	JANS1N6485
JAN1N6485C	JANTX1N6485C	JANTXV1N6485C	JANS1N6485C
JAN1N6485CUS	JANTX1N6485CUS	JANTXV1N6485CUS	JANS1N6485CUS
JAN1N6485D	JANTX1N6485D	JANTXV1N6485D	JANS1N6485D
JAN1N6485DUS	JANTX1N6485DUS	JANTXV1N6485DUS	JANS1N6485DUS
JAN1N6485US	JANTX1N6485US	JANTXV1N6485US	JANS1N6485US
JAN1N6486	JANTX1N6486	JANTXV1N6486	JANS1N6486
JAN1N6486C	JANTX1N6486C	JANTXV1N6486C	JANS1N6486C
JAN1N6486CUS	JANTX1N6486CUS	JANTXV1N6486CUS	JANS1N6486CUS
JAN1N6486D	JANTX1N6486D	JANTXV1N6486D	JANS1N6486D
JAN1N6486DUS	JANTX1N6486DUS	JANTXV1N6486DUS	JANS1N6486DUS
JAN1N6486US	JANTX1N6486US	JANTXV1N6486US	JANS1N6486US
JAN1N6487	JANTX1N6487	JANTXV1N6487	JANS1N6487
JAN1N6487C	JANTX1N6487C	JANTXV1N6487C	JANS1N6487C
JAN1N6487CUS	JANTX1N6487CUS	JANTXV1N6487CUS	JANS1N6487CUS
JAN1N6487D	JANTX1N6487D	JANTXV1N6487D	JANS1N6487D
JAN1N6487DUS	JANTX1N6487DUS	JANTXV1N6487DUS	JANS1N6487DUS
JAN1N6487US	JANTX1N6487US	JANTXV1N6487US	JANS1N6487US

* 6.6 List of PINs – continued.

JAN1N6488	JANTX1N6488	JANTXV1N6488	JANS1N6488
JAN1N6488C	JANTX1N6488C	JANTXV1N6488C	JANS1N6488C
JAN1N6488CUS	JANTX1N6488CUS	JANTXV1N6488CUS	JANS1N6488CUS
JAN1N6488D	JANTX1N6488D	JANTXV1N6488D	JANS1N6488D
JAN1N6488DUS	JANTX1N6488DUS	JANTXV1N6488DUS	JANS1N6488DUS
JAN1N6488US	JANTX1N6488US	JANTXV1N6488US	JANS1N6488US
JAN1N6489	JANTX1N6489	JANTXV1N6489	JANS1N6489
JAN1N6489C	JANTX1N6489C	JANTXV1N6489C	JANS1N6489C
JAN1N6489CUS	JANTX1N6489CUS	JANTXV1N6489CUS	JANS1N6489CUS
JAN1N6489D	JANTX1N6489D	JANTXV1N6489D	JANS1N6489D
JAN1N6489DUS	JANTX1N6489DUS	JANTXV1N6489DUS	JANS1N6489DUS
JAN1N6489US	JANTX1N6489US	JANTXV1N6489US	JANS1N6489US
JAN1N6490	JANTX1N6490	JANTXV1N6490	JANS1N6490
JAN1N6490C	JANTX1N6490C	JANTXV1N6490C	JANS1N6490C
JAN1N6490CUS	JANTX1N6490CUS	JANTXV1N6490CUS	JANS1N6490CUS
JAN1N6490D	JANTX1N6490D	JANTXV1N6490D	JANS1N6490D
JAN1N6490DUS	JANTX1N6490DUS	JANTXV1N6490DUS	JANS1N6490DUS
JAN1N6490US	JANTX1N6490US	JANTXV1N6490US	JANS1N6490US
JAN1N6491	JANTX1N6491	JANTXV1N6491	JANS1N6491
JAN1N6491C	JANTX1N6491C	JANTXV1N6491C	JANS1N6491C
JAN1N6491CUS	JANTX1N6491CUS	JANTXV1N6491CUS	JANS1N6491CUS
JAN1N6491D	JANTX1N6491D	JANTXV1N6491D	JANS1N6491D
JAN1N6491DUS	JANTX1N6491DUS	JANTXV1N6491DUS	JANS1N6491DUS
JAN1N6491US	JANTX1N6491US	JANTXV1N6491US	JANS1N6491US

6.7 Changes from previous issue. The margins of this specification are marked with astericks to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the previous issue.

Custodians:
Army - CR
Navy - EC
Air Force - 85
NASA - NA
DLA - CC

Preparing activity:
DLA - CC

(Project 5961-2015-030)

Review activities:
Army - AR, MI, SM
Navy - AS, MC
Air Force - 19

NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at https://assist.dla.mil .